uDSim, a Microprocessor Design Time

Simulation infrastructure

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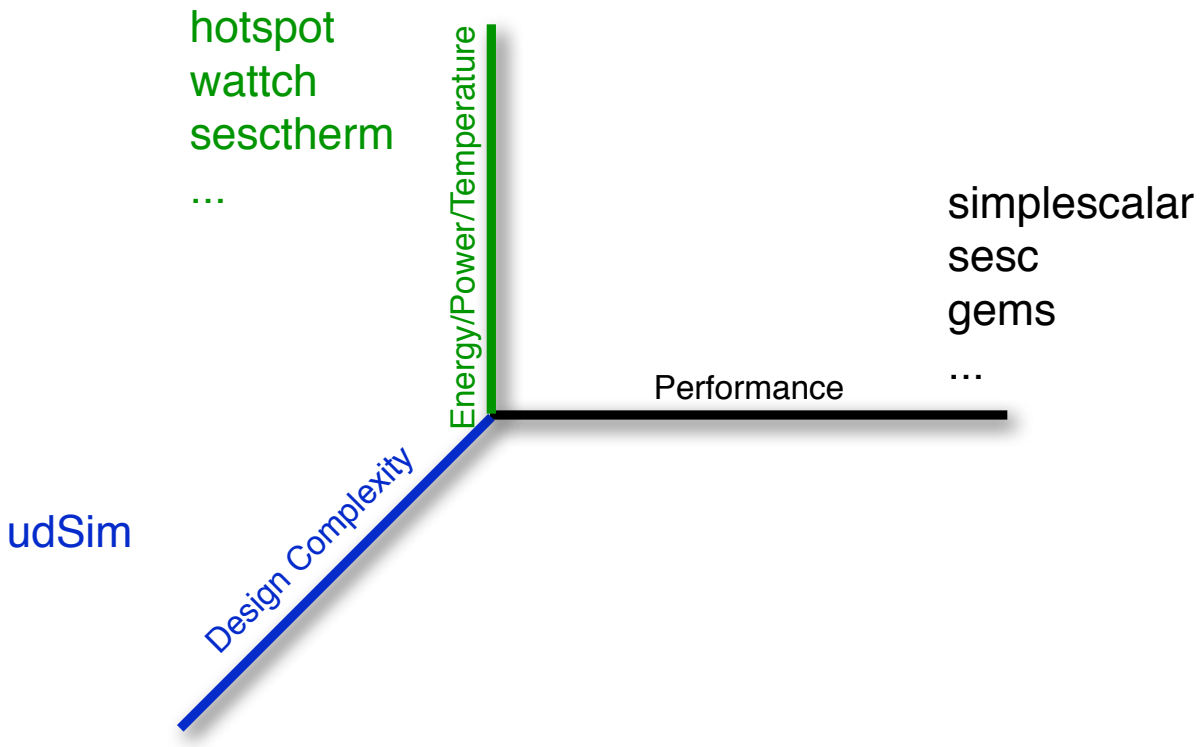
Design Space Exploration

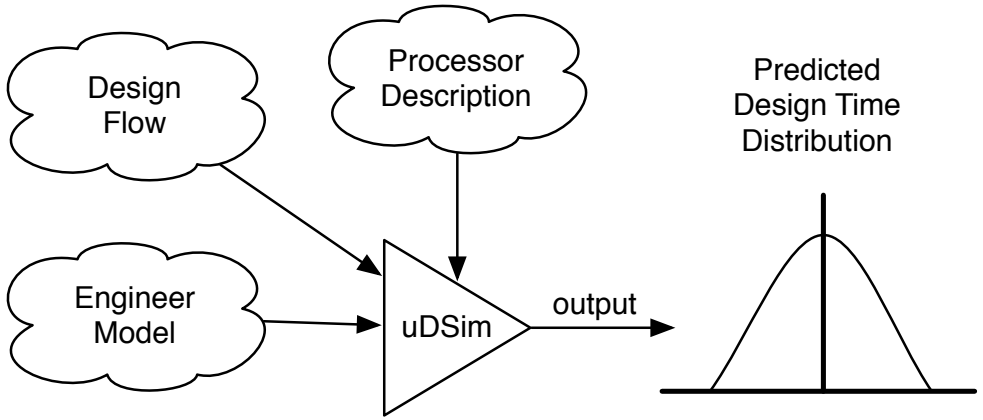


Objective

- Capacity to compare design times across proposals
  - E.g:
    - Compare design times for LSQ-A or LSQ-B

Key Factors

- Architectural proposal characteristics
- Design workflow
- Engineers



Potential Show Stoppers

- How do you model engineers?
- How much detail is enough?
  - Sickness, coffee, restroom...
  - Communication, meetings...
  - Different productivity
  - ...
- What about bugs?
- How do you validate your model?

Modeling Engineers

- Just keep it simple, basic parameters. Use existing data:
  - Different engineer skills
  - Productivity increases with time
  - Model communication
  - Bugs created are proportional to work hours
- It can be done as an event driven simulator
  - Similarities to an architectural simulator
    - Multiple engineers interact (Instead of CPUs)
    - Work minutes are the product (Instead of retired instructions)
    - Events: communication, bugs, productivity increase
  - A key difference
    - Not deterministic. Need to do Monte-Carlo simulations

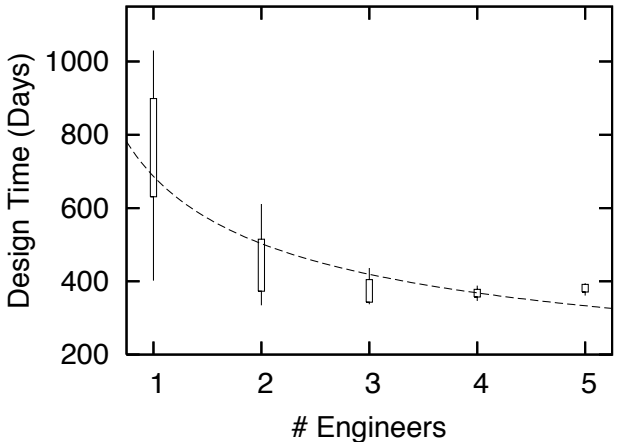
Validation I

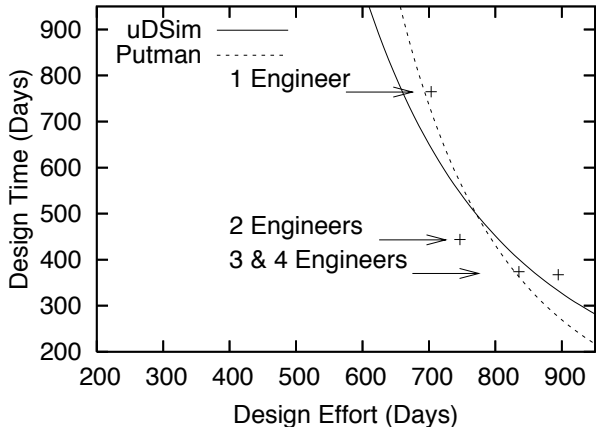
- Compare with existing CPU designs
  - Currently for 13 samples, we have 0.97 correlation

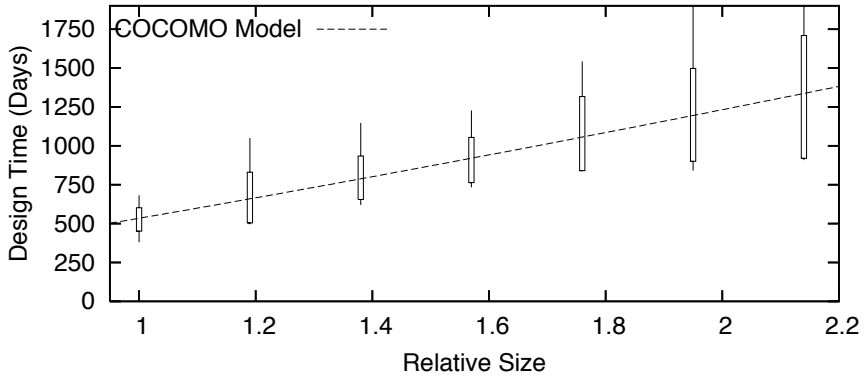
Processor Block	Reported	udSim Time
PUMA-Fetch	60	49
PUMA-Decode	80	89
PUMA-ROB	80	99
PUMA-Execute	240	226
PUMA-Memory	20	18

Validation II

- Make sure that it follows software engineering models







Sample Utilization

- Estimate design time for an issue logic proposal
  - SEED [Martinez et al PACT06]
- Original paper
  - Frequency, area, and power improvements
- Replaced the Illinois Verilog Model (EV6-like) for SEED
  - 8% total design time increase or 1.5 additional months

Conclusions

- Sounds WACI to predict “human design time”
  - but it yields very good results with very few parameters (5)
- First time to use a simulation to estimate design time
  - Not used by software engineering
- **Contact me if you have data for any large project**

Questions?

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