SCOORE

Santa Cruz Out-of-Order Risc Engine

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OVERVIEW

SCOORE is a high performance Out-of-Order SPARC V8 processor currently under implementation by the MASC research lab at UCSC.

SCOORE has several novel aspects; it is an Out-of-Order implementation of the SPARC V8 ISA, it is also being developed with full FPGA and ASIC compatibility as a major design goal. In comparison with current Intel and AMD processors, SCOORE has a larger Issue Logic, Reorder Buffer (ROB), and Register File size. Design specifications call for an operating frequency of 1.4 GHz on 90 nm ASIC, and 175 MHz on an FPGA.

FPGA IMPLEMENTATION

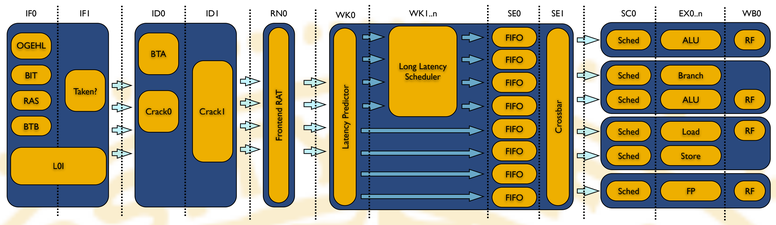
SCOORE is being used as a development platform to define a set of guidelines for FPGA-friendly Out-of-Order CPU designs. An Out-of-Order CPU completely implementable on an FPGA has not yet been efficiently achieved. This is a valuable feature that allows researchers to perform realistic evaluations and simulations.

XUPV5-LX110T

Nallatech FSB

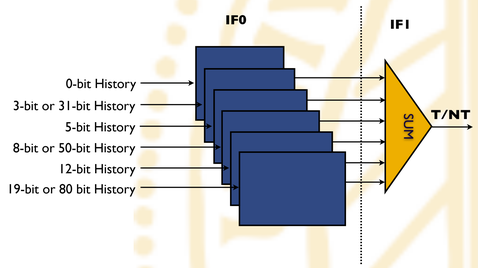
- Xilinx Virtex-5
- XUP Board
  - DDR2 SODIMM
  - Shared Board with OpenSPARC
  - Full System
- Nallatech FSB
  - X86 Host Boots Linux

- 1.4 GHz ASIC Frequency
- Efficient FPGA Synthesis
- 2 Way SMP



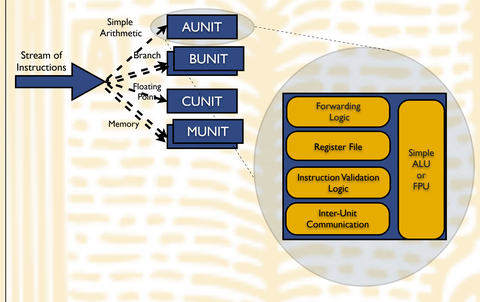
- 4-Issue Superscalar
- SPARC V8 Processor
- Out-of-Order Execution

INSTRUCTION FETCH



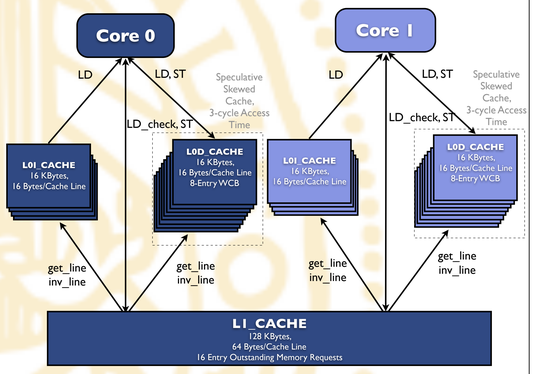
- 100 Kbits OGEHL predictor
  - 6 Table Predictor
  - Variable Branch History: 0 to 80 bits
  - Speculative Update with Fixup
- 4 KByte direct map BTB prediction
  - 2 Predictions per Cycle
- 32-entry RAS predictor

COMPUTE ENGINE

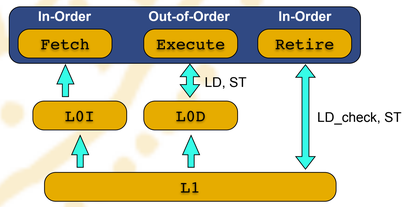


- 4 Cluster Implementation
  - AUNIT: Arithmetic Unit (1 port)
    - Simple Arithmetic
  - BUNIT: Branch Unit (2 ports)
    - Branches/Arithmetic
  - CUNIT: Complex Unit (1 port)
    - Floating Point, mult, div
  - MUNIT: Memory Unit (2 ports)
    - Load/Store

MEMORY SUBSYSTEM



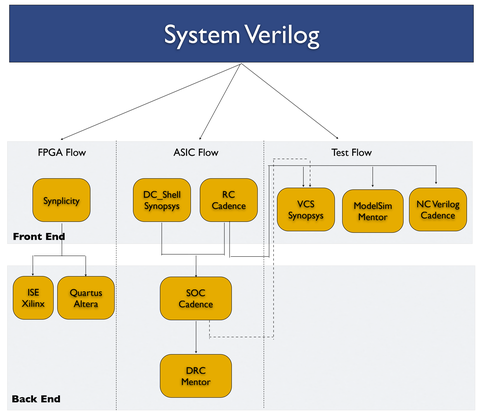
- Memory Speculation
  - LD/ST Execute Out-of-Order
  - LD/ST Re-execute In-Order for Verification



TARGETS

	FPGA		ASIC					
UNIT	LUTS	RAMS	AREA (COMB) (mm²)	SRAM AREA (mm²)	MAXIMUM POWER (mW)	LEADERS	STATUS	ESTIMATED COMPLETION DATE
BPRED	2,000	12	0.10	0.70	200	Tom	60%	1Q'10
CRACK/DECODE	5,000	2	0.20	0.10	300	Carlos	35%	2Q'10
L0I CACHE	2,000	8	0.10	0.20	200	Tom	95%	2Q'10
L0D CACHE	7,000	12	0.30	0.70	500	David/Anupam	80%	1Q'10
SCHEDULER	17,000	4	0.20	0.70	500	Abhishek/Elnaz	95%	3Q'09
RAT/ROB	25,000	8	0.60	0.70	500	Gregory	5%	1Q'10
SELECT	5,000	2	0.20	0.00	200	Elnaz	40%	4Q'09
FPU	7,000	2	0.30	0.00	200	Rigo	90%	4Q'09
COMPUTE ENGINE	35,000	18	1.40	1.20	1,000	Rigo	70%	3Q'09
L1 CACHE	12,000	40	0.50	3.00	3,000	David/Anupam	5%	2Q'10
TOTAL	**117,000**	**108**	**3.90**	**7.30**	**6,900**			**2Q '10**

DESIGN FLOW



GOALS / MILESTONES

- Summer 2009
  - Complete AUNIT, CUNIT
  - Implement Extensive Testbenches
  - Implement BUNIT, MUNIT
  - Integrate the Scheduler
- Fall 2009
  - Integrate the RAT/ROB
  - FPGA Preparation

FUTURE RESEARCH

This project will serve as an infrastructure to advance research and education in micro-architectural topics such as: simulation, thermal modeling, thermal validation, architectural pruning, design complexity analysis, and hardware bug realization.

- Add Thread Level Speculation
- Implement 'Pruned' Versions of SCOORE
- Boot µCLinux

The design and implementation of SCOORE has been a completely collaborative effort. It has been used extensively in undergraduate and graduate courses as a practical teaching tool. In addition to the previous and current students at MASC, thanks to all CMPE 202 and CMPE 125 students who participated in this project. Funding provided by NSF, NASA, Sun Microsystems, and Xilinx.