CHAPTER 5

COMPUTER ORGANIZATION

WE NOW TAKE A MORE ABSTRACT VIEW IN OUR STUDY OF COMPUTER SYSTEMS. RATHER THAN FOCUS ON THE MOST ELEMENTARY COMPONENTS (TRANSISTORS, GATES, ETC.), WE STUDY COMPUTERS AS COLLECTIONS OF FUNCTIONAL UNITS OR SUBSYSTEMS WHICH PERFORM SPECIFIC TASKS SUCH AS: INSTRUCTION PROCESSING, DATA STORAGE, DATA TRANSFER, INPUT/OUTPUT.

VON NEUMAN ARCHITECTURE

JOHN VON NEUMAN (1903-1957) WAS ONE OF THE GREATEST MATHEMATICIANS OF THIS CENTURY. HE MADE FUNDAMENTAL CONTRIBUTIONS TO THEORETICAL PHYSICS, ECONOMICS, GAME THEORY, PURE MATHEMATICS, AND COMPUTER SCIENCE.

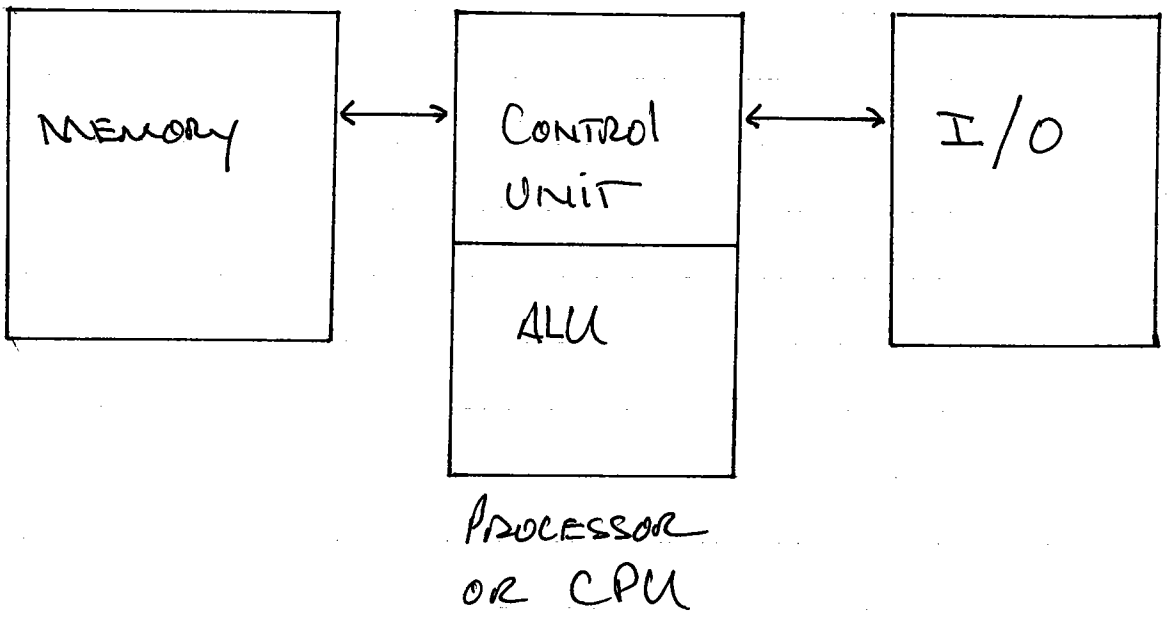
VIRTUALLY ALL MODERN COMPUTERS TODAY (PC, MAINFRAME, LAPTOP, PDA) ARE BASED ON A SINGLE DESIGN MODEL CALLED THE VON NEUMAN ARCHITECTURE, FIRST PROPOSED IN 1946.

THIS DESIGN HAS THREE CHARACTERISTICS:

- FOUR MAJOR SUBSYSTEMS :
  1.) MEMORY
  2.) INPUT/OUTPUT
  3.) ARITHMETIC/LOGIC UNIT (ALU)
  4.) CONTROL UNIT

- THE STORED PROGRAM CONCEPT
  ALGORITHM INSTRUCTIONS ARE STORED IN MEMORY ENCODED AS SEQUENCES OF BINARY NUMBERS

- SEQUENTIAL EXECUTION OF INSTRUCTIONS
  INSTRUCTIONS ARE FETCHED FROM MEMORY, ONE AT A TIME, TO THE CONTROL UNIT WHERE THEY ARE DECODED AND EXECUTED.



MEMORY

ALL INSTRUCTIONS AND DATA ARE STORED INTERNALLY IN BINARY FORM. THE MEMORY UNIT ITSELF IS OFTEN CALLED RANDOM ACCESS MEMORY (RAM). IT HAS THE FOLLOWING CHARACTERISTICS.

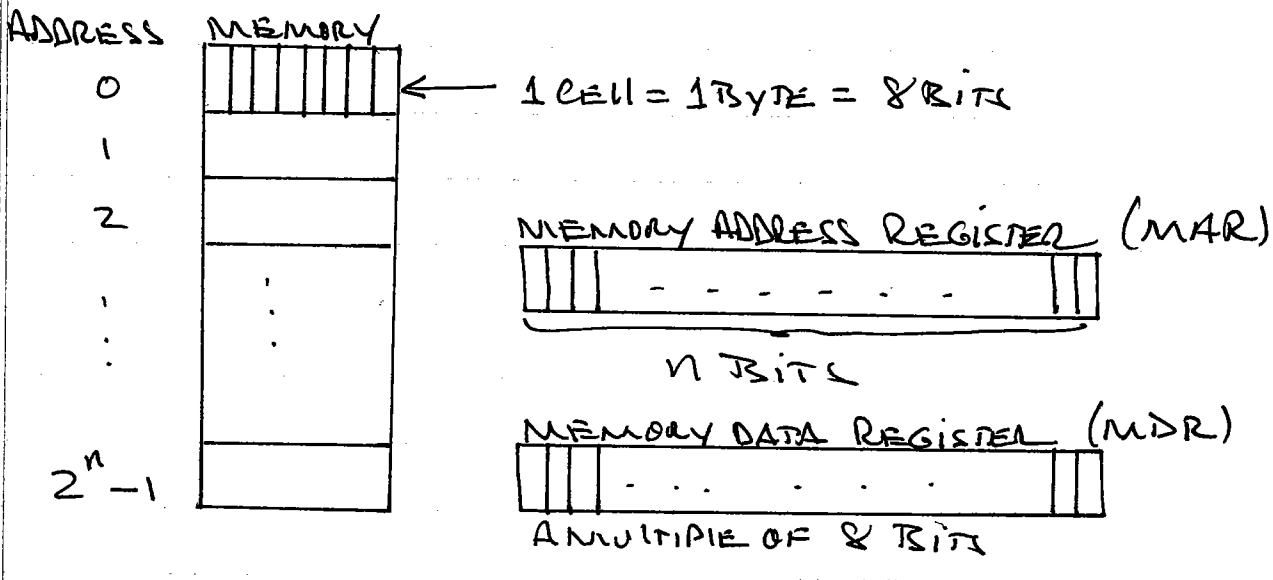
- MEMORY IS DIVIDED INTO CELLS OF A FIXED SIZE (i.e. NUMBER OF BITS.) EACH CELL IS ASSOCIATED WITH A UNIQUE UNSIGNED INTEGER CALLED ITS ADDRESS. THE FIXED SIZE OF EACH CELL IS CALLED THE CELL WIDTH. THE UNIVERSALLY ACCEPTED VALUE FOR THIS WIDTH IS 8 BITS, ALSO CALLED A BYTE.

- THERE ARE TWO BASIC MEMORY OPERATIONS CALLED FETCH AND STORE WHICH ARE PERFORMED ON AN ENTIRE CELL.

- THE TIME IT TAKES TO ACCESS A CELL IS THE SAME FOR ALL CELLS IN MEMORY. (HENCE RANDOM ACCESS.)

OFTEN A SINGLE DATA VALUE OCCUPIES MULTIPLE BYTES OF STORAGE. SEVERAL TRIPS TO MEMORY WOULD BE REQUIRED TO FETCH AN INTEGER, SAY. SOME TYPICAL STORAGE REQUIREMENTS ARE:

- CHARACTER (ASCII): 1 BYTE
- INTEGER: 2, 4 BYTES
- REAL NUMBER: 4 or 8 BYTES.



THE MEMORY ADDRESS REGISTER (MAR) HOLDS THE ADDRESS OF THE CELL WHICH IS ABOUT TO BE FETCHED OR STORED. IF THE MAR CONTAINS n BITS THEN THERE CAN BE AT MOST 2^n BYTES OF ADDRESSABLE MEMORY. THE ADDRESSES MAY RANGE FROM 0 TO

$$\underbrace{1111\cdots11}_{n} = 2^n - 1 .$$

IT IS IMPORTANT TO KEEP IN MIND THE DIFFERENCE BETWEEN A CELL'S ADDRESS AND A CELL'S CONTENTS.

EX $n = 6$, $\therefore$ AT MOST $2^6 = 64$ CELLS

ADDRESS	CONTENTS
011010	10110100
26	172

64 BYTES IS A SMALL AMOUNT OF MEMORY. A TYPICAL VALUE FOR n WOULD BE 16 - 32

MEMORY IS OFTEN MEASURED IN KILOBYTES AND MEGABYTES, HOWEVER A KILOBYTE IS NOT 1000 BYTES.

1 BYTE = 8 BITS
1 KB = 2^{10} BYTES = 1,024 BYTES
1 MB = 2^{20} " = 1,048,576 "
1 GB = 2^{30} " = 1,073,741,824 "
1 TB = 2^{40} " = 1,099,511,627,776.

EX. 128 MB = 2^7 MB = $2^7 \cdot 2^{20} = 2^{27}$ BYTES.

$\therefore$ 2^{27} ADDRESSABLE CELLS
$\therefore$ $n \geq 27$.

THE MEMORY DATA REGISTER (MDR) CONTAINS THE DATA VALUE WHICH IS ABOUT TO BE FETCHED OR STORED. SINCE MOST DATA VALUES OCCUPY MORE THAN ONE CELL, THE SIZE OF THE MDR IS USUALLY SOME MULTIPLE OF THE CELL WIDTH (1 BYTE). TYPICALLY THE MDR IS 16, 32, OR 64 BITS WIDE.

THE FETCH AND STORE OPERATIONS CAN BE DESCRIBED AS FOLLOWS:

FETCH (ADDRESS)

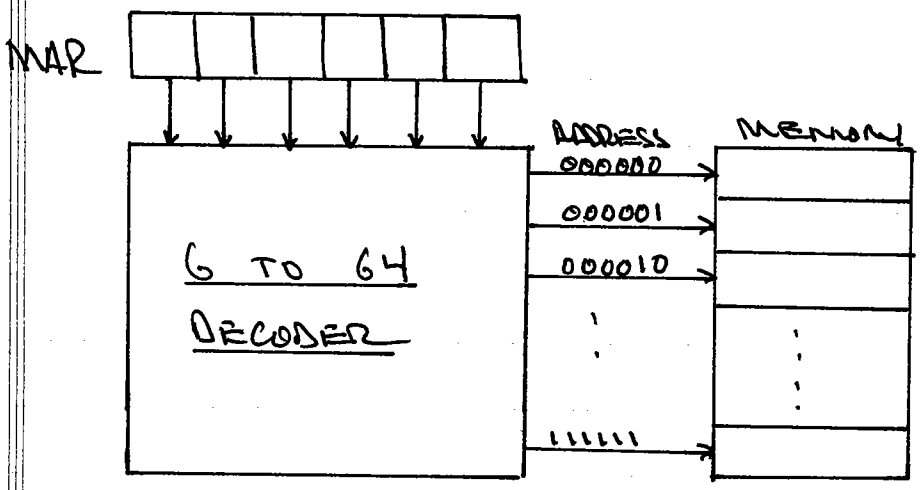
1.) LOAD ADDRESS INTO MAR
2.) DECODE ADDRESS IN MAR
3.) COPY CONTENTS OF CELL TO MDR

STORE (ADDRESS, VALUE)

1.) LOAD ADDRESS INTO MAR
2.) LOAD VALUE INTO MDR
3.) DECODE ADDRESS IN MAR
4.) COPY CONTENTS OF MDR INTO CELL

THE "DECODE ADDRESS" STEP IN THESE ALGORITHMS IS IMPLEMENTED USING THE DECODER CIRCUIT OF THE LAST CHAPTER.

EX. $n = 6$, $\therefore 2^6 = 64$ ADDRESSABLE CELLS.



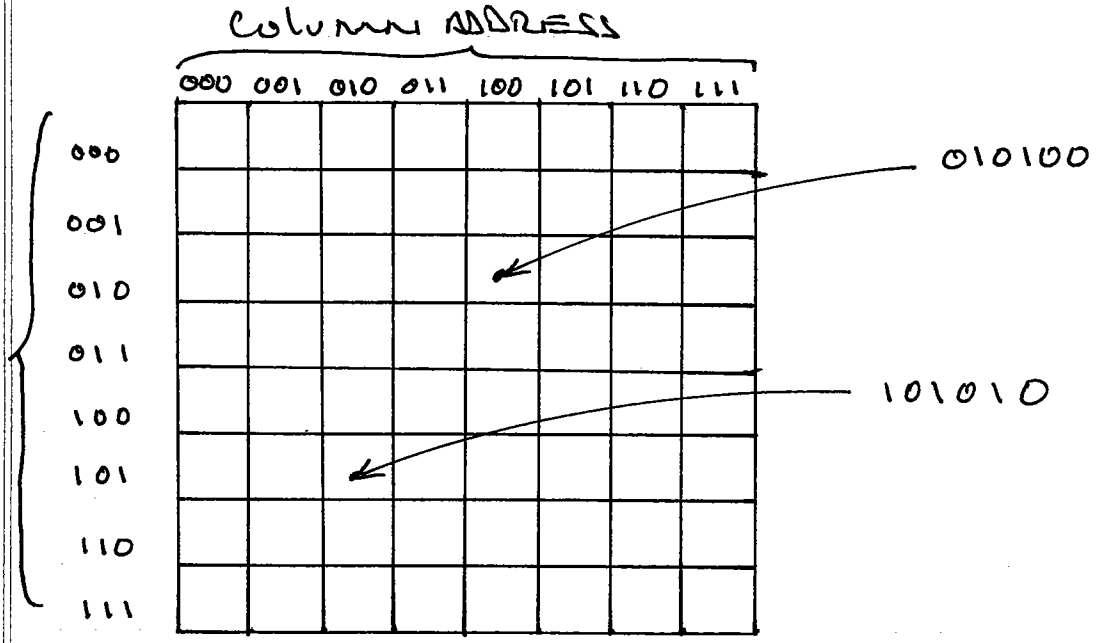
IF FOR INSTANCE THE MAR CONTAINS 001101 = 13, THEN THE OUTPUT LABELED 13 WILL BE ON, ENABLEING CELL 13 TO BE FETCHED OR STORED.

A MORE REALISTIC MEMORY SIZE WOULD BE 16 MB = $2^4 \cdot 2^{20} = 2^{24}$ BYTES. THUS $n = 24$, AND WE WOULD HAVE TO BUILD A 24 TO $2^{24} = 16,777,216$ DECODER.

FORTUNATELY THIS IS NOT NECESSARY SINCE MEMORY DEVICES ARE 2-DIMENSIONAL, RATHER THAN 1-DIMENSIONAL.

EACH CELL IS AT THE INTERSECTION OF A UNIQUE ROW AND COLUMN. THE CELL'S ADDRESS IS THEN ITS ROW ADDRESS FOLLOWED BY ITS COLUMN ADDRESS.

Ex $n=6$, 2^6 cells $= 2^3$ rows $\times$ 2^3 columns.



INSTEAD OF ONE 6 TO 64 DECODER WE CAN BUILD TWO 3 TO 8 DECODERS.