THE CIRCUIT RETURNS THE CORRECT ANSWER AS LONG AS

$$[a_{n-1} \cdots a_0] \geq [b_{n-1} \cdots b_0]$$

IN WHICH CASE THE FINAL BORROW BIT IS 0; OTHERWISE THE FINAL BORROW IS 1.

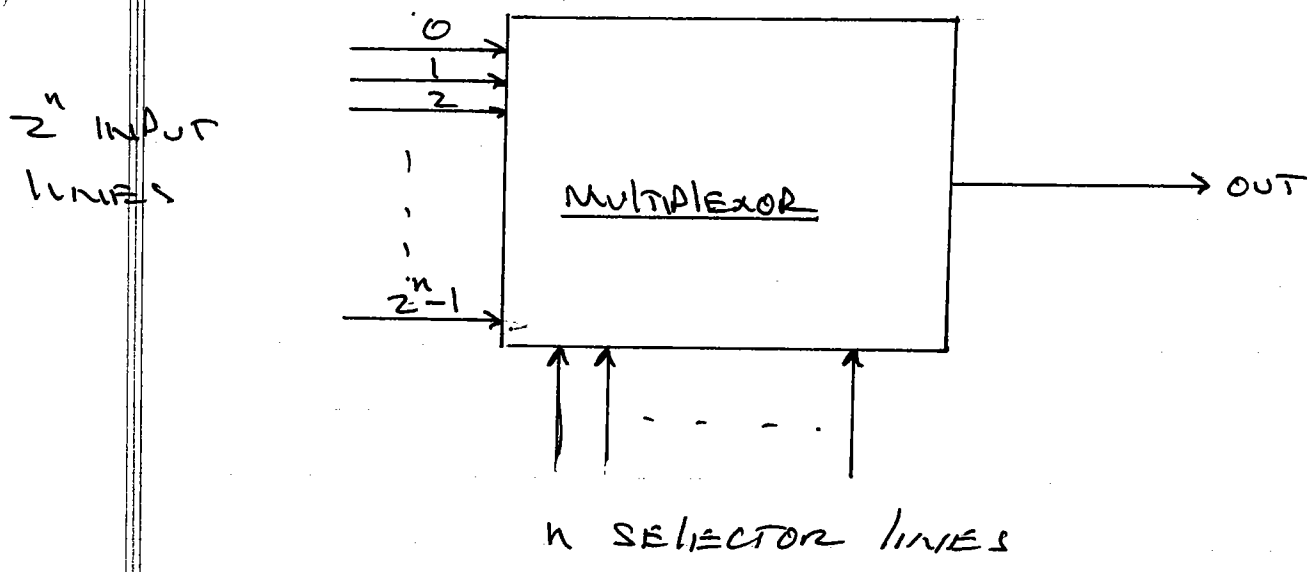
CONTROL CIRCUITS

SO FAR WE'VE LOOKED ONLY AT CIRCUITS THAT IMPLEMENT ARITHMETIC AND LOGIC FUNCTIONS.

CONTROL CIRCUITS ARE USED TO DETERMINE WHICH OPERATIONS ARE TO BE PERFORMED, AND TO SELECT THE CORRECT DATA VALUES TO BE PROCESSED.

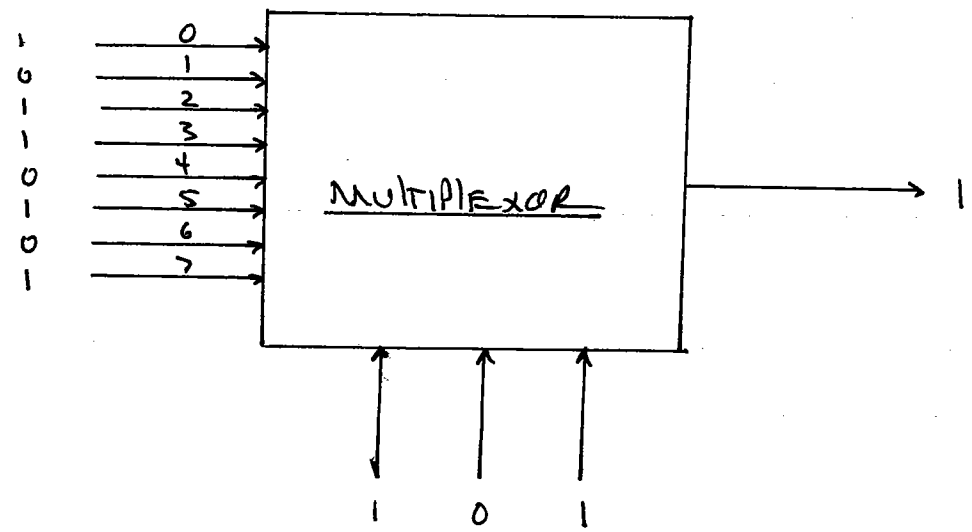
THE TWO TYPES OF CONTROL CIRCUITS WE WILL STUDY ARE MULTIPLEXORS AND DECODERS.

A MULTIPLEXOR HAS 2^n "INPUT" LINES, n SELECTOR LINES ($\therefore 2^n + n$ TOTAL INCOMING LINES) AND 1 OUTPUT LINE.



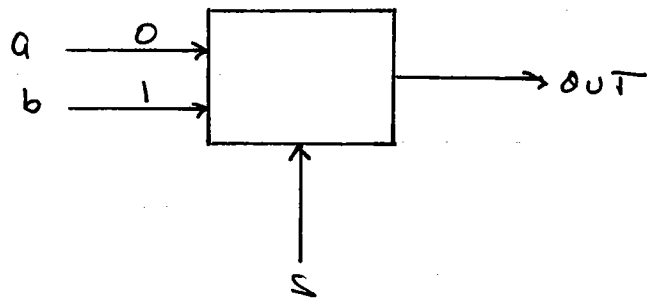
THE 2^n INPUT LINES ARE LABELED $0, 1, \ldots, 2^n - 1$. THE FUNCTION OF THE MULTIPLEXOR IS TO SELECT ONE OF ITS INPUT LINES, AND SEND THAT BIT TO ITS OUTPUT LINE. IT DOES THIS BY LOOKING AT THE n BITS ON ITS SELECTOR LINES AND INTERPRETING THIS AS AN INTEGER IN THE RANGE 0 TO $2^n - 1$.

EX. $n = 3$



WITH $8+3=11$ INPUT LINES, THE TRUTH TABLE FOR THIS CIRCUIT WOULD HAVE $2^{11} = 2048$ ROWS!

Ex. $n=1$



THE TRUTH TABLE FOR THE 2-INPUT MULTIPLEXOR IS

a	b	s	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

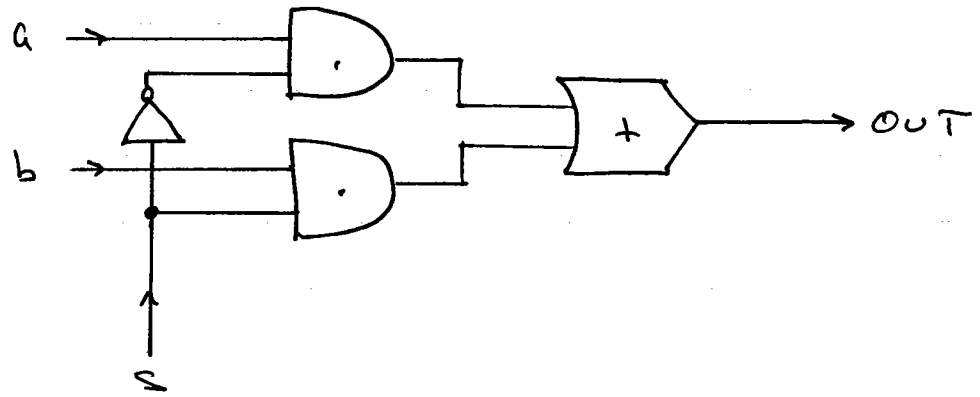
$$\therefore \quad OUT \equiv (\bar{a}\cdot b\cdot s)+(a\cdot \bar{b}\cdot \bar{s})+(a\cdot b\cdot \bar{s})+(a\cdot b\cdot s)$$

THIS EXPRESSION LEADS TO A RATHER COMPLICATED CIRCUIT, WHICH CAN BE SIMPLIFIED CONSIDERABLY.

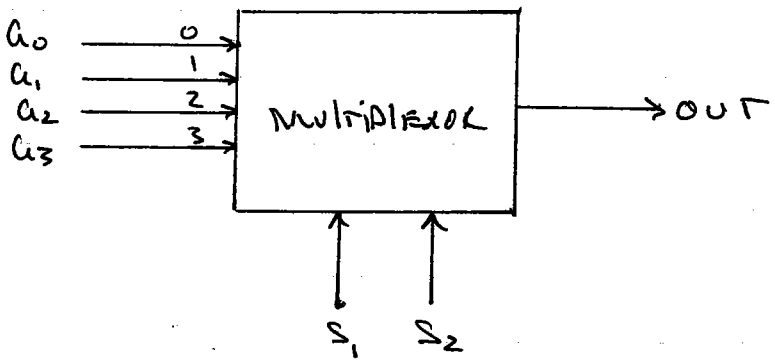
ONE CHECKS USING TRUTH TABLES THAT

$$OUT \equiv (a \cdot \bar{s}) + (b \cdot s)$$

WHICH LEADS TO THE FOLLOWING OPTIMAL CIRCUIT:



HW PROBLEM 19 (P.167) ASKS THAT YOU DESIGN A 4-INPUT MULTIPLEXOR. THUS $n=2$ AND THERE ARE $2^n+n = 6$ LINES COMING IN TO THIS CIRCUIT, AND $2^6 = 64$ ROWS IN ITS TRUTH TABLE. THE RESULTING "SUM OF PRODUCTS" EXPRESSION LEADS TO A <u>VERY</u> COMPLICATED CIRCUIT.



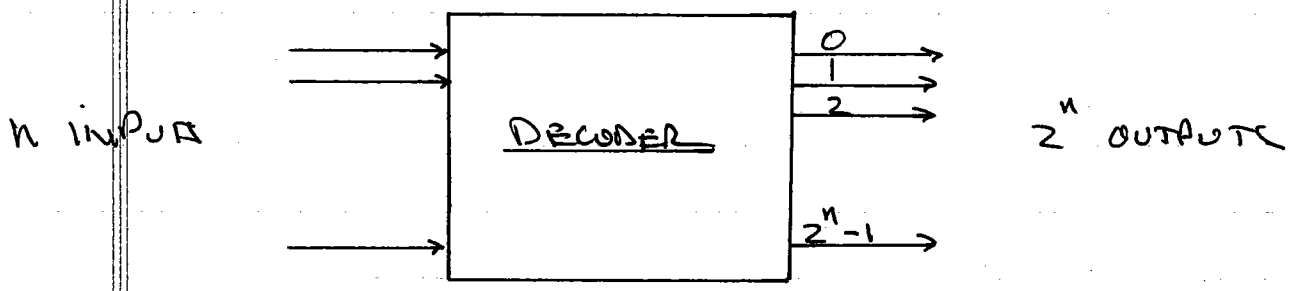
THIS IS <u>NOT</u> THE APPROACH TO TAKE.

INSTEAD CONSIDER THE FOLLOWING EXPRESSION:

$$(a_0 \cdot \bar{S}_1 \cdot \bar{S}_2) + (a_1 \cdot \bar{S}_1 \cdot S_2) + (a_2 \cdot S_1 \cdot \bar{S}_2) + (a_3 \cdot S_1 \cdot S_2)$$

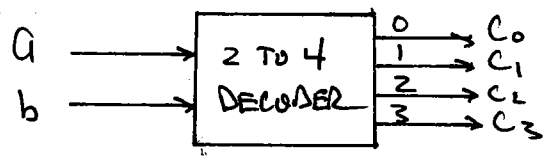
DOES THIS RELATIVELY SIMPLE EXPRESSION GIVE THE CORRECT TRUTH TABLE?

A <u>DECODER</u> IS (IN SOME SENSE) AN INVERSE TO A MULTIPLEXOR. IT HAS n INPUT LINES AND 2^n OUTPUT LINES LABELED 0 TO $2^n - 1$.



THE n INPUT BITS ARE INTERPRETED AS A BINARY NUMBER IN THE RANGE 0 TO $2^n - 1$. THE CORRESPONDING OUTPUT LINE IS THEN SET TO 1 AND ALL OTHERS ARE SET TO 0.

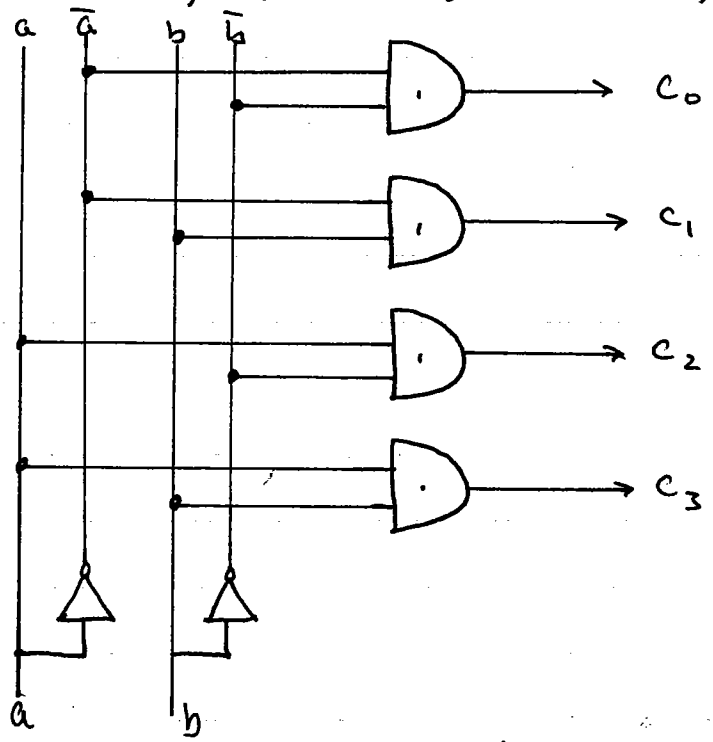
<u>EX.</u> $n = 2$. $2^2 = 4$ OUTPUTS



TRUTH TABLE:

a	b	c_0	c_1	c_2	c_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$\therefore c_0 \equiv \bar{a} \cdot \bar{b}$, $c_1 \equiv \bar{a} \cdot b$, $c_2 \equiv a \cdot \bar{b}$, $c_3 \equiv a \cdot b$



IN PROBLEM 20 YOU DESIGN A 3 TO 8 DECODER.

HW4: CHAP 4 P. 166:

1 abc, 3 abcd, 4, 5 abc, 6b, 7 abc, 8 bcd, 9, 11 abcd

HW5: CHAP 4 P. 166:

13, 14, 15, 16, 18, 19, 20