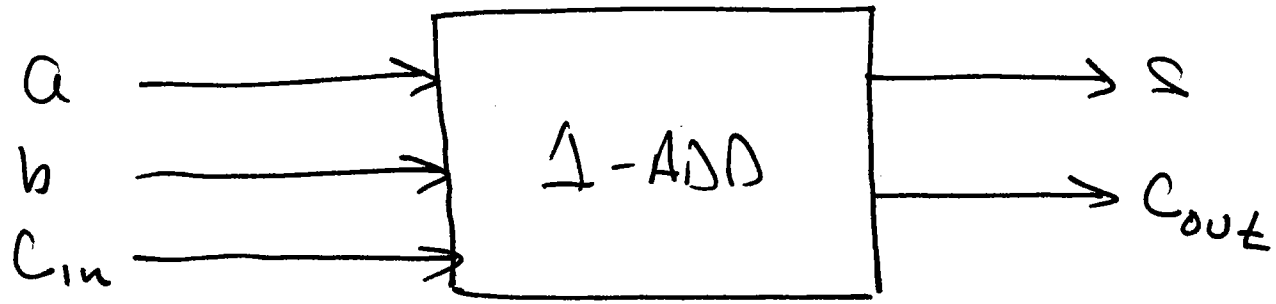
CMPS 10 2-21-08

GOAL: DESIGN AN N-BIT FULL ADDER.

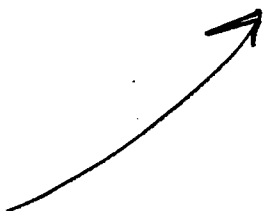
FIRST: DESIGN A 1-BIT ADDER



47 TRANSISTORS

$$c_{out} \equiv (\bar{a} \cdot b \cdot c) + (a \cdot \bar{b} \cdot c) + (a \cdot b \cdot \bar{c}) + (a \cdot b \cdot c)$$

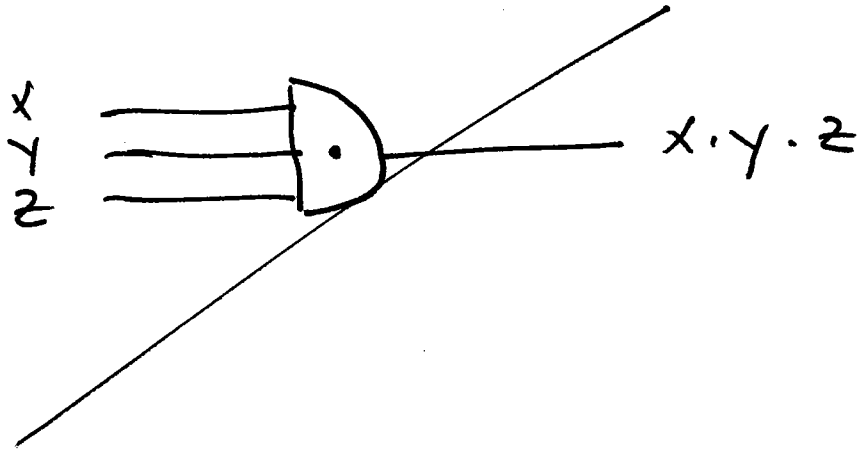
$$\equiv [(\bar{a} \cdot \bar{b} \cdot c) + (\bar{a} \cdot b \cdot \bar{c})] + [(a \cdot \bar{b} \cdot \bar{c}) + (a \cdot b \cdot c)]$$

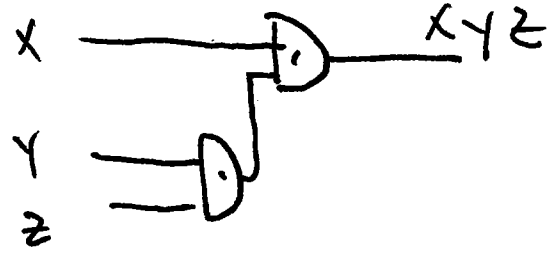


SUM-OF-PRODUCT EXPRESSIONS FOR c_{out} & s FROM TRUTH TABLE.

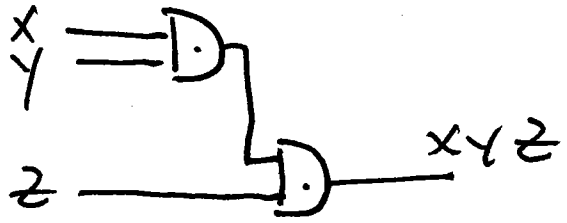
SEE P. 89 OF NOTES FOR CIRCUIT.

NOTE: There is NO 3-input and gate.





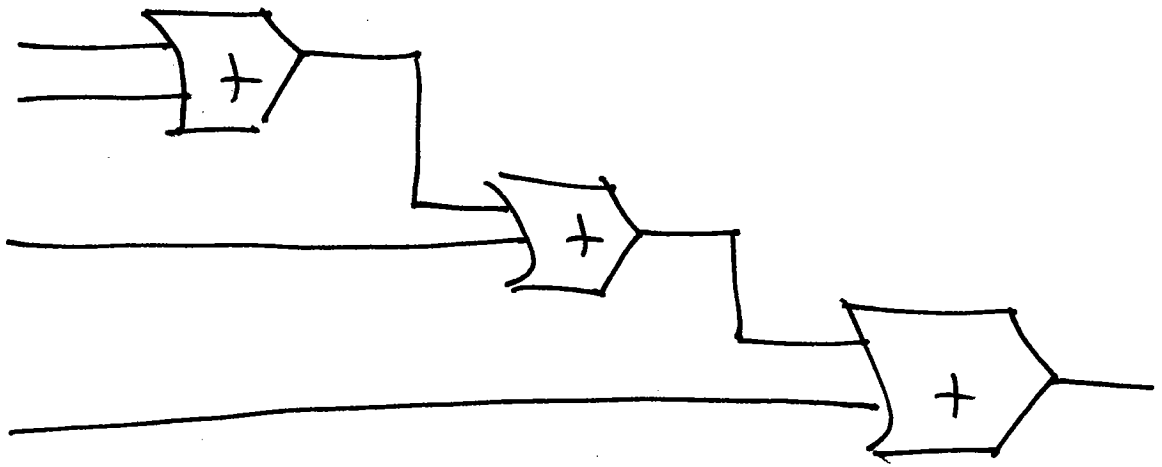
or



$$x \cdot (y \cdot z) \equiv (x \cdot y) \cdot z$$

Could Also DO

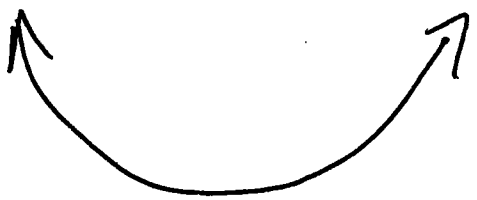
$$S = ((\bar{a}\bar{b}c + \bar{a}b\bar{c}) + a\bar{b}\bar{c}) + abc$$



Thm: $x(yz) \equiv (xy)z$

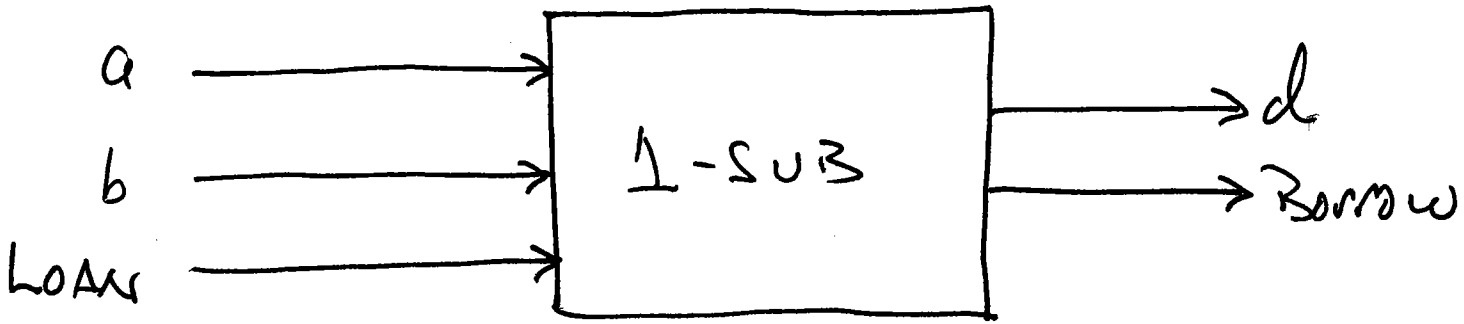
$$x + (y+z) \equiv (x+y) + z$$

x	y	z	x·y	(x·y)·z	(y·z)	x·(y·z)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1



EX. SUBTRACTION.

$$\begin{array}{cccc} {\scriptstyle 0}\ {\scriptstyle 1}\ {\scriptstyle 0} & & & \\ X\ X\ 0 & 1 & = & 13 \\ 0 & 1 & 1 & 1 \\ \hline 0 & 1 & 1 & 0 \end{array} \quad \begin{array}{c} \\ \\ = \\ \hline = \end{array} \quad \begin{array}{c} \\ \\ 7 \\ \hline 6 \end{array}$$



$$\text{Borrow} = \begin{cases} 1 \text{ if } a-b-\text{loan} < 0 \\ 0 \text{ if } a-b-\text{loan} \geq 0 \end{cases}$$

$$d = 2.\text{Borrow} + a - b - \text{loan}$$

TRUTH TABLE

a	b	loan	d	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logical Expressions:

$$d \equiv \bar{a}\bar{b}l + \bar{a}b\bar{l} + a\bar{b}\bar{l} + abl$$

$$\text{Borrow} \equiv \bar{a}\bar{b}l + \bar{a}b\bar{l} + \bar{a}bl + abl$$

Exercise: Draw the circuit.

transistors = 47

CONTROL CIRCUIT :

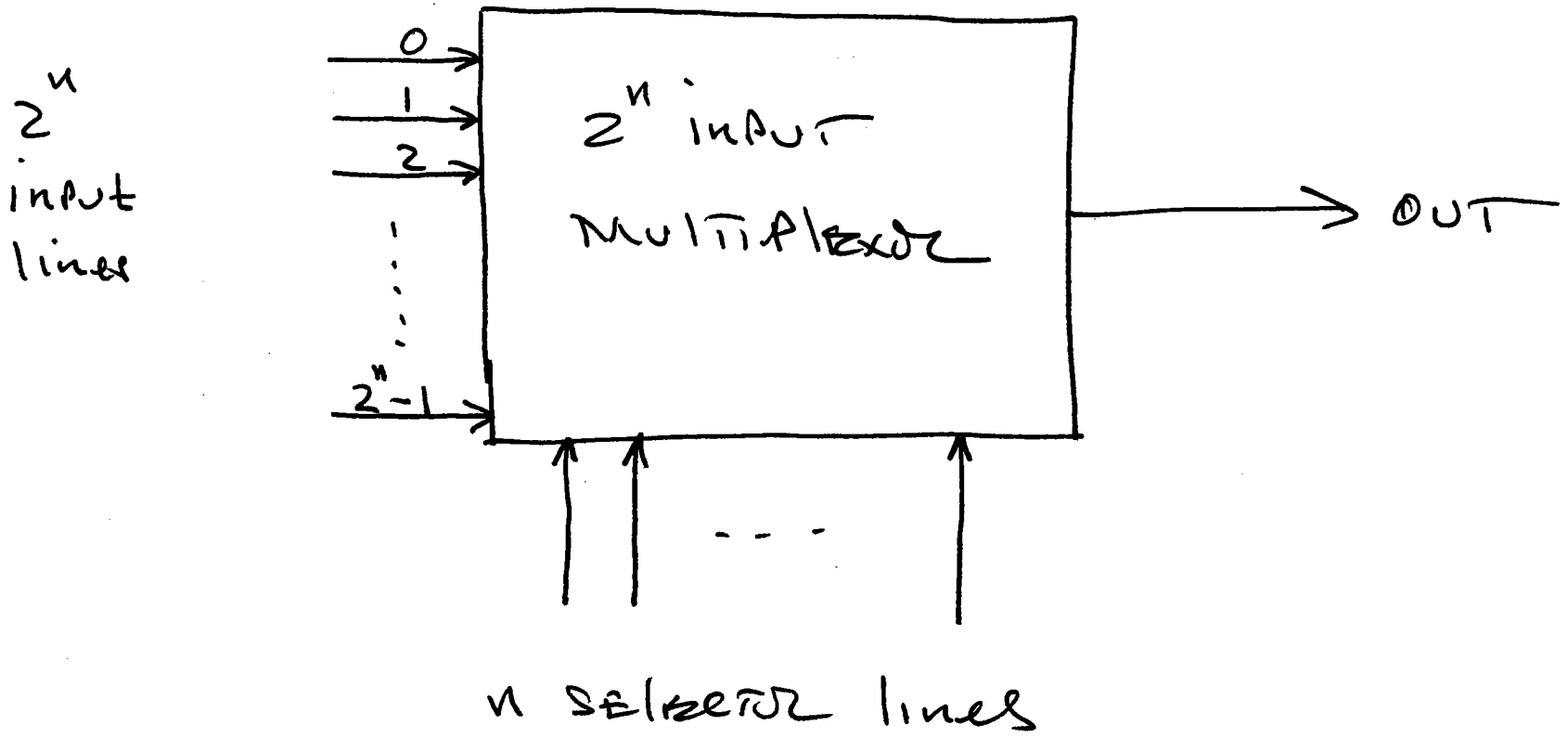
- MULTIPLEXER
- DECODER

MULTIPLEXER :

2^n 'INPUT lines' } $2^n + n$ INDEPENDENT INPUTS

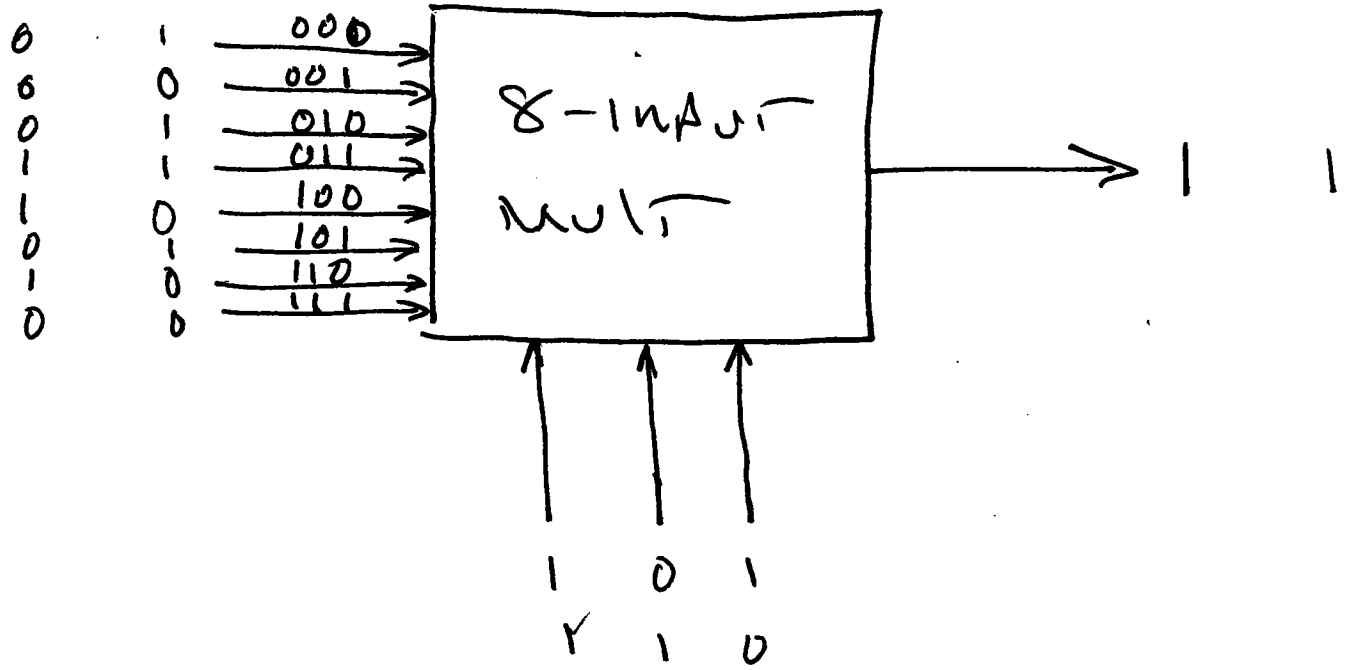
n SELECTOR lines }

1 OUTPUT line.



This circuit selects the input line whose label is identical to the bit string on the n selector lines, and copies it to OUT.

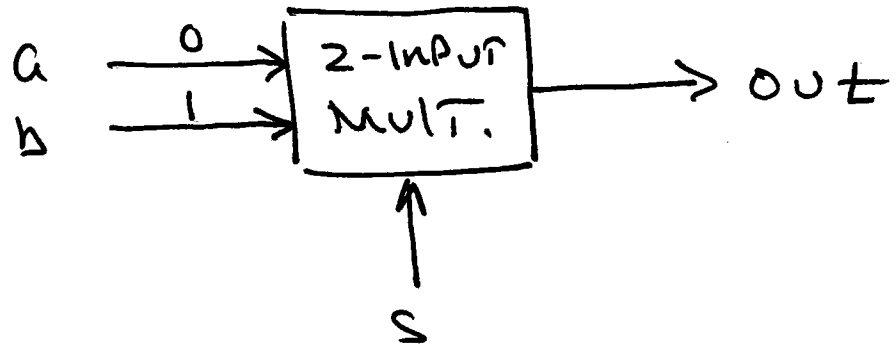
Ex. $n=3$



INP. INPUTS = 11

ROWS = 2^{11} = 2048

Ex $n = 1$ # inputs $= 3$, $\therefore$ # rows $= 8$



a	b	s	out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

LOGICAL EXPRESSION:

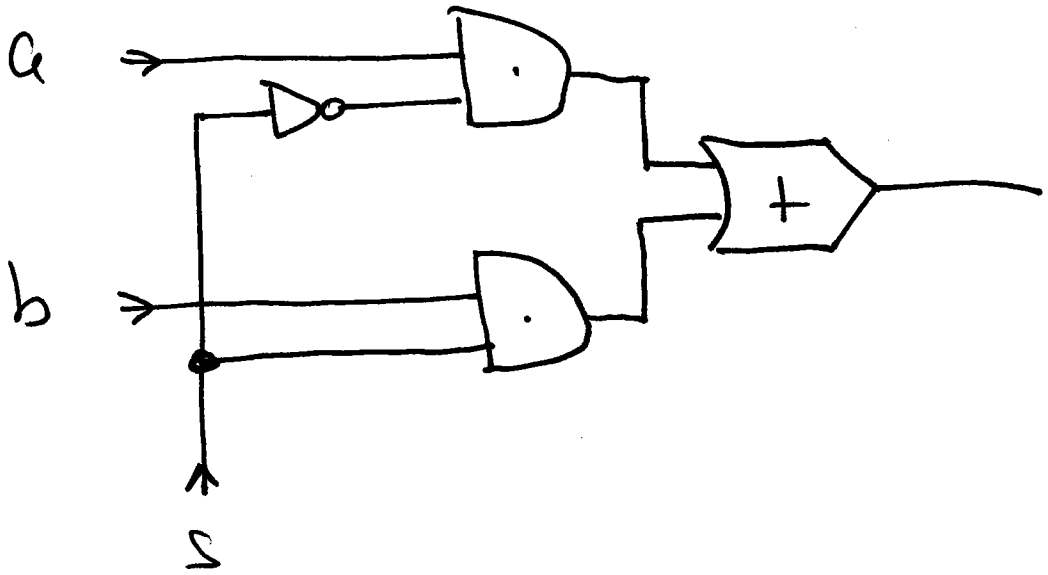
$$OUT \equiv \bar{a}bs + a\bar{b}\bar{s} + ab\bar{s} + abs$$

SIMPLIFIED EXPRESSION:

$$OUT \equiv a\bar{s} + bs$$

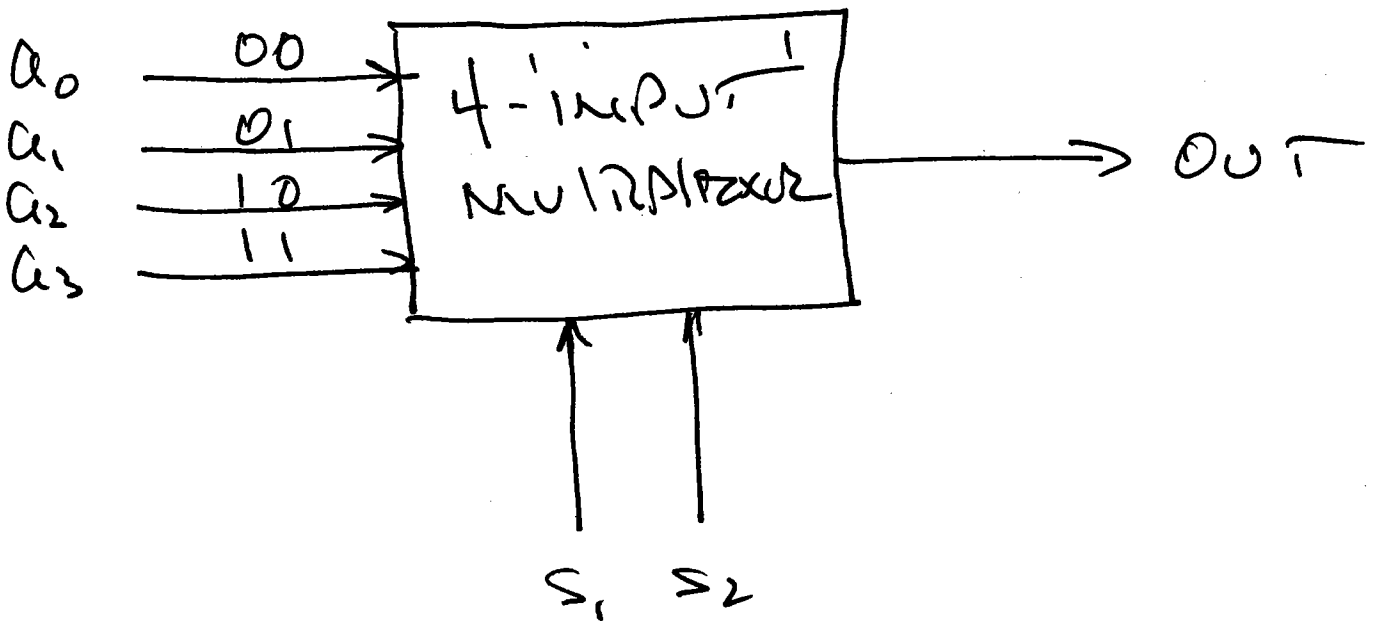
a	b	s	$\bar{s}$	$a\bar{s}$	bs	$a\bar{s} + bs$
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	0	0	0
1	1	0	1	1	0	1
1	1	1	0	0	1	1

circuit.



Prob. #23 on p. 180 asks for a 4-input multiplexor.

i.e. $n = 2$



Consider

$$OUT \equiv a_0(\bar{S}_1, \bar{S}_2) + a_1(\bar{S}_1, S_2) + a_2(S_1, \bar{S}_2) + a_3(S_1, S_2)$$

00 01 10 11