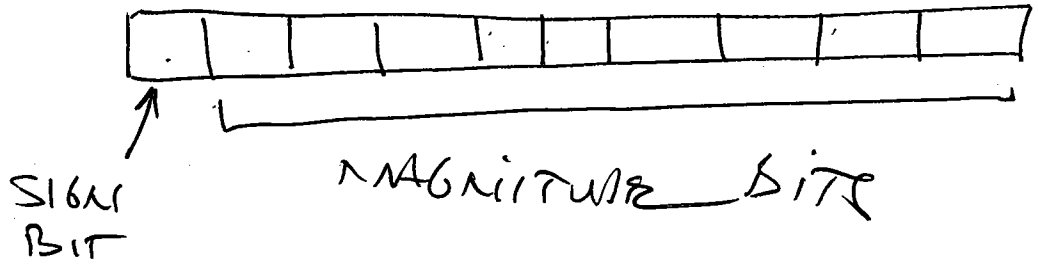
CMPS 10 2-14-08

SIGN/MAGNITUDE REPRESENTATION OF SIGNED INTEGERS.

EX. USE 10 BITS FOR S/MAG REP.



RANGE: $1\ 111111111 = -(2^9 - 1) = -511$

TO

$0\ 111111111 = +(2^9 - 1) = +511$

of #s = 1023

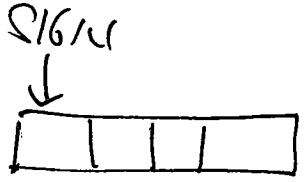
of bit strings of length 10 $= 2^{10} = 1024$

Problem 2 Representations of 0 !

0 0000000000

1 0000000000

Ex. Same but use 4 bits:



Range: -7 to +7, # of #s = 15

(# of bit strings of length 4) $= 2^4 = 16$

Two's Complement Representation of Signed Integers.

Ex. Again using 4 bits for signed integers

Dec	Two's Comp. Rep.
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
-8	1000
-7	1001
-6	1010
-5	1011
-4	1100
-3	1101
-2	1110
-1	1111

$$\begin{array}{r} 2 = 0010 \\ +\ 3 = 0011 \\ \hline 5 = 0101 \end{array}$$

$$\begin{array}{r} 2 = 0010 \\ +\ (-6) = 1010 \\ \hline (-4) = 1100 \end{array}$$

To Negate: Flip Bits & Add 1

$$5 \quad 0101 \rightarrow 1010 \rightarrow 1011 \quad -5$$

~~1~~ 1

Try $5 = 0101$

$(-2) = 1110$

$3 = 0011$

WHAT ABOUT FRACTIONAL i.e. #s WITH A FRACTIONAL PART ?

EX. 12.75

EX. $-0.21093 75$

EX. 17.125

FLOATING POINT REPRESENTATION

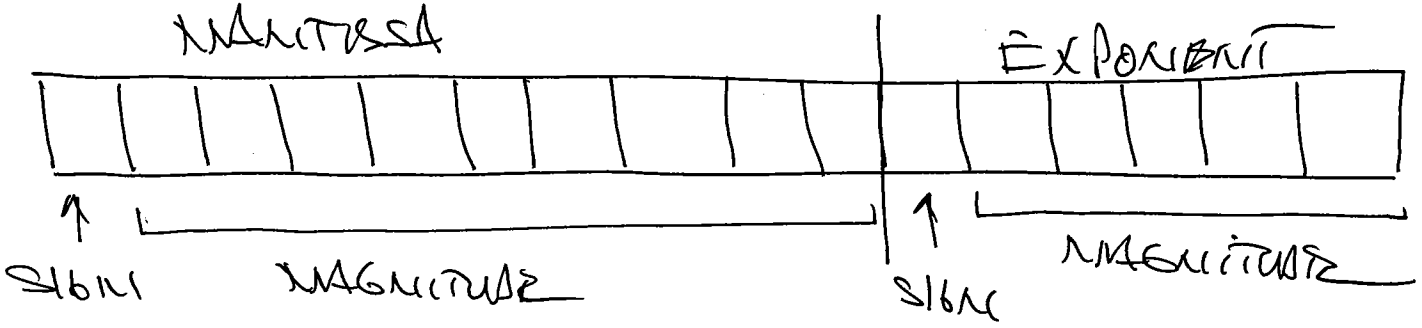
- FIRST CONVERT TO SCIENTIFIC NOTATION

$$\pm M \cdot 2^{\pm E}$$

  - $\pm M$: SIGNED INTEGER: MANTISSA
  - $\pm E$: SIGNED INTEGER: EXPONENT

- STORE BITS FOR $\pm M$ & $\pm E$

EX ASSUME WE USE 16 BITS FOR F.P. REP WITH 10 BITS FOR MANTISSA, 6 BITS FOR EXP.

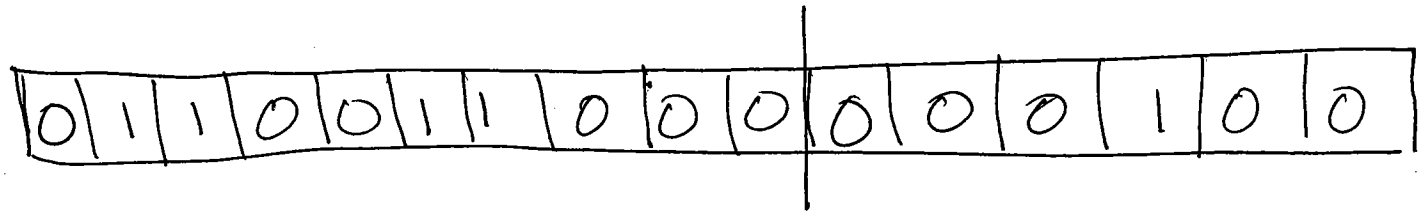


Ex. $12.75^{-} = 8+4+\frac{1}{2}+\frac{1}{4} = 2^3+2^2+2^{-1}+2^{-2}$

$= [1100.11]_2$

$= [.110011]_2 \cdot 2^{+4}$

$= +[.110011]_2 \cdot 2^{+[100.]_2}$



Ex. -0.2109375

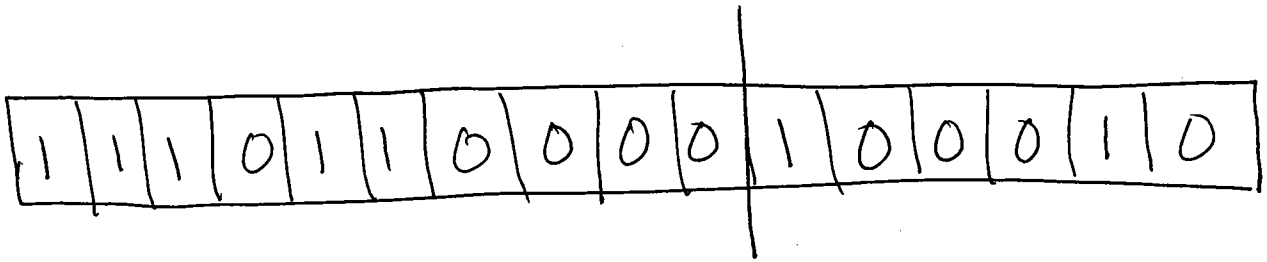
$$= -\left(\frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{128}\right)$$

$$= -\left(2^{-3} + 2^{-4} + 2^{-6} + 2^{-7}\right)$$

$$= -[.0011011]_2$$

$$= -[.11011]_2 \cdot 2^{-2} = -[.11011] \cdot 2^{-[10]_2}$$

SAMPLE ASSUMPTION: 16 BITS { 10 BIT MANTISSA, 6 " EXP.



TEXT DATA

EACH CHARACTER IS REPRESENTATION BY A CHARACTER CODE, i.e. A NUMBER

ENCODING SCHEMES:

- ASCII USES 8 BITS PER CHAR
- UNICODE USES 16 BITS PER CHAR

→ $256 = 2^8$ CHAR CODES: 00000000 [0] TO 11111111 [255]

32-126 ARE ASSIGNED TO PRINTABLE CHARS. (P. 128 SEC 4.3)

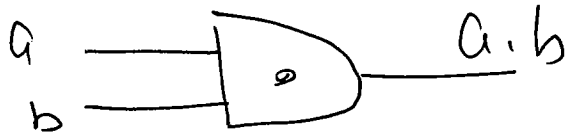
Why Binary? Reliability

BISTABLE DEVICE: TRANSISTOR.

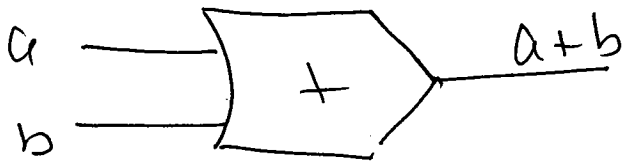
LOGIC GATES:

NOTATION:

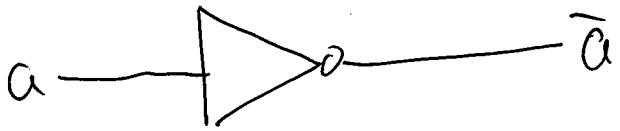
a and b	$\approx$	$a \wedge b$	$\approx$	$a \cdot b$
a or b	$\approx$	$a \vee b$	$\approx$	$a + b$
not a	$\approx$	$\neg a$	$\approx$	$\overline{a}$
ENGLISH		MATH		CIRCUITS



a	b	a · b
0	0	0
0	1	0
1	0	0
1	1	1



a	b	a + b
0	0	0
0	1	1
1	0	1
1	1	1



a	ā
0	1
1	0