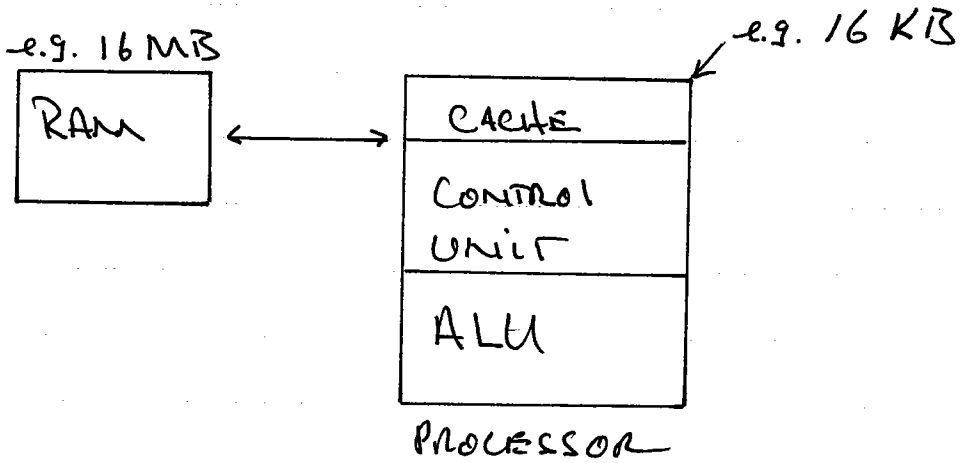
BACK TO MORE REALISTIC NUMBERS: 16 MB $= 2^{24}$ BYTES $= 2^{12}$ ROWS $\times$ 2^{12} COLUMNS. INSTEAD OF ONE 24 TO 16,777,216 DECODER, WE BUILD TWO 12 TO $2^{12} = 4096$ DECODERS.

THE MEMORY UNIT ALSO CONTAINS A DEVICE CALLED THE FETCH/STORE CONTROLLER WHICH DETERMINES WHETHER A FETCH OR STORE OPERATION WILL BE PERFORMED. (SEE FIG. 5.7 P. 182)

CACHE MEMORY

IN ADDITION TO THE MAIN MEMORY DEVICE MODERN PROCESSORS HAVE AN ADDITIONAL STORE OF VERY FAST MEMORY CALLED CACHE.



CACHE MEMORY IS MADE WITH EXPENSIVE FABRICATION TECHNIQUES AND CAN BE ACCESSED AT RATES UP TO 10 TIMES FASTER THAN RAM.

WHEN AN ITEM IS NEEDED FROM MEMORY, THE PROCESSOR FIRST LOOKS IN CACHE. IF THE ITEM IS THERE, IT IS ACCESSED AT THE FASTER RATE. IF NOT, IT IS FETCHED FROM RAM AT THE SLOWER RATE. THE ITEM IS THEN PLACED IN CACHE, OVERWRITING AN OLDER ITEM.

THIS DESIGN IS BASED ON THE <u>PRINCIPLE OF LOCALITY</u>, WHICH SAYS THAT IF THE PROCESSOR USES AN ITEM, IT WILL PROBABLY USE IT AGAIN SOON.

<u>EX.</u>
SUPPOSE THE ITEM NEEDED IS IN CACHE 70 % OF THE TIME. (THIS IS CALLED THE <u>CACHE HIT RATE</u>.) SUPPOSE CACHE ACCESS TIME IS 10 NS, WHILE RAM TAKES 50 NS TO ACCESS. THE AVERAGE ACCESS TIME IS THEN

$$(.70)\cdot 10 + (.30)(50+10) = 25 \text{ NSEC.},$$

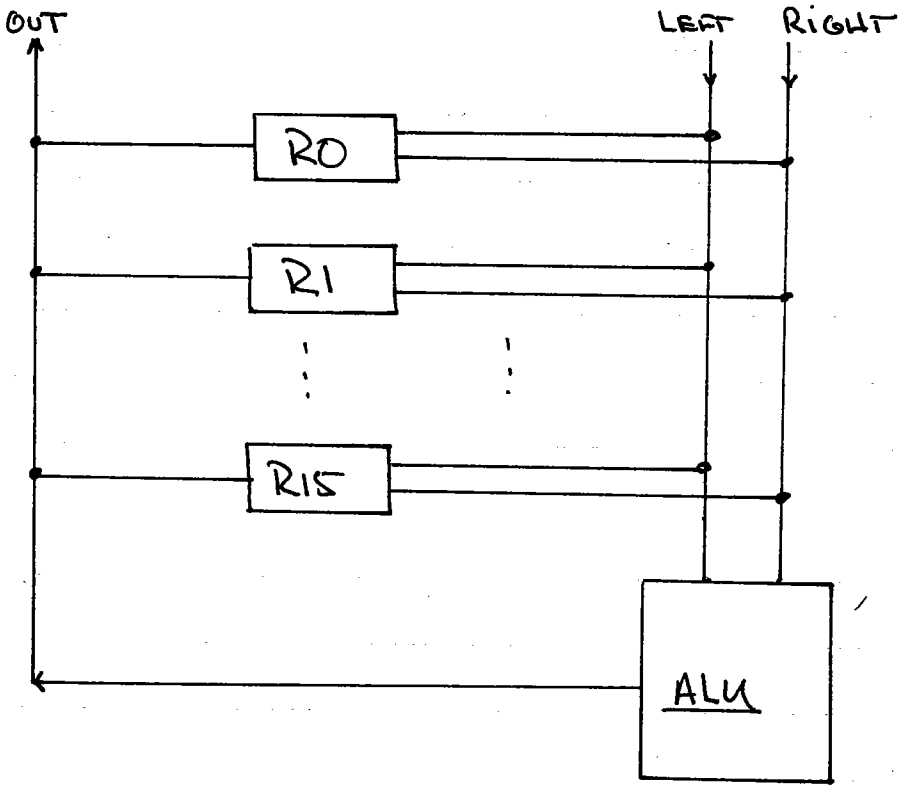
A 50 % IMPROVEMENT OVER 50 NSEC FOR RAM.

- <u>READ</u> 5.2.2 I/O & MASS STORAGE
  P. 184 - 189

THE ARITHMETIC/LOGIC UNIT (ALU)

THE ALU IS THE SUBSYSTEM WHICH PERFORMS MATHEMATICAL & LOGICAL OPERATIONS SUCH AS ADDITION, SUBTRACTION, COMPARISON, ETC..

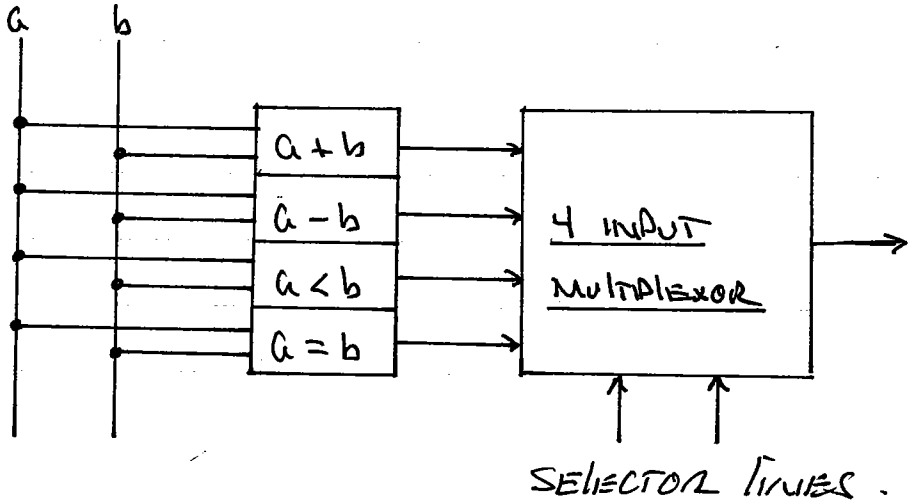
IN ADDITION TO THE CIRCUITRY WHICH PERFORMS THESE OPERATIONS THE ALU CONTAINS A NUMBER OF REGISTERS. THESE ARE SPECIAL STORAGE CELLS WHICH HOLD THE OPERANDS OF UPCOMING OPERATIONS, AS WELL AS INTERMEDIATE RESULTS. A TYPICAL ALU WILL HAVE 16-32 REGISTERS. THESE ARE SIMILAR TO CACHE MEMORY IN THAT THEY ALLOW VERY FAST ACCESS.



TO PERFORM AN OPERATION, THE OPERANDS ARE FIRST MOVED FROM RAM TO THE ALU REGISTERS. ONE REGISTER IS CONNECTED TO THE BUS LABELED LEFT, THE OTHER TO THE BUS LABELED RIGHT. (A BUS IS SIMPLY AN ELECTRICAL DATA PATH WHICH "STOPS" AT A NUMBER OF LOCATIONS.) THE ALU IS THEN ENABLED TO PERFORM THE DESIRED OPERATION. THE RESULT IS PASSED TO THE OUTPUT BUS, AND IS EITHER PLACED IN ANOTHER REGISTER, OR LEAVES THE ALU.

HOW DOES THE ALU KNOW WHICH OPERATION TO PERFORM? ONE APPROACH IS TO HAVE THE ALU PERFORM ALL OPERATIONS, THEN USE A MULTIPLEXOR TO SELECT THE OUTPUT.

EX. SUPPOSE OUR ALU DOES JUST FOUR OPERATIONS:
$a+b$, $a-b$, $a<b$, $a=b$.



NOTE THAT IN THESE DIAGRAMS, A SINGLE LINE CAN REPRESENT 8 OR MORE SEPARATE ELECTRICAL PATHS. THIS IS IN KEEPING WITH THE LARGER SCALE, ABSTRACT VIEW WE ARE TAKING. WE WILL GLOSS OVER MANY SUCH DETAILS.

THE CONTROL UNIT

RECALL A FUNDAMENTAL CHARACTERISTIC OF THE VON NEUMAN ARCHITECTURE IS THE STORED PROGRAM: A SEQUENCE OF INSTRUCTIONS STORED AS BINARY VALUES IN MEMORY.

IT IS THE TASK OF THE CONTROL UNIT TO:

1.) FETCH THE NEXT INSTRUCTION
2.) DECODE THE INSTRUCTION
3.) EXECUTE THE INSTRUCTION

UNTIL A SPECIAL INSTRUCTION (e.g. HALT) IS ENCOUNTERED. STEPS (1)-(3) CAN BE THOUGHT OF AS THE BODY OF A REPEAT LOOP.

STORED PROGRAM INSTRUCTIONS ARE ENCODED IN A REPRESENTATION CALLED MACHINE LANGUAGE.

A TYPICAL FORMAT FOR A MACHINE LANGUAGE INSTRUCTION WOULD CONSIST OF AN OPERATION CODE FOLLOWED BY ONE OR MORE ADDRESS FIELDS.

THE OPERATION CODE (OP-CODE) IS A UNIQUE UNSIGNED INTEGER CODE ASSIGNED TO EACH OPERATION WHICH THE PROCESSOR CAN PERFORM.

THE ADDRESS FIELDS CONTAIN THE MEMORY ADDRESSES OF THE OPERANDS. EACH ADDRESS FIELD MUST BE THE SAME WIDTH AS THE MAR.

EX. INSTRUCTION REGISTER (IR)

OP CODE	ADDR1	ADDR2	ADDR3
8	24	24	24

BITS:

WHEN AN INSTRUCTION IS FETCHED FROM MEMORY IT IS PLACED IN A SPECIAL LOCATION CALLED THE INSTRUCTION REGISTER (IR)

IN THIS EXAMPLE EACH INSTRUCTION OCCUPIES 10 BYTES OF MEMORY, WHICH IS THE WIDTH OF THE IR. THERE ARE AT MOST 2^8 = 256 OPERATIONS, AND THE MEMORY UNIT CONTAINS AT MOST 2^{24} BYTES = 16 MB.

THE SET OF ALL OPERATIONS WHICH CAN BE PERFORMED BY A PROCESSOR IS CALLED ITS <u>INSTRUCTION SET</u>.

COMPLEX INSTRUCTION SET COMPUTERS (CISC) RECOGNIZE 200 - 400 OPERATIONS, REDUCED INSTRUCTION SET COMPUTERS (RISC) RECOGNIZE ABOUT 30 - 50 OPERATIONS.

THE TREND IN RECENT YEARS HAS BEEN TOWARDS RISC PROCESSORS WHICH RUN FASTER THAN CISC DESIGNS. THE TRADE OFF IS TO HAVE LONGER, MORE COMPLEX MACHINE LANGUAGE PROGRAMS. THIS HAS BECOME MORE ACCEPTABLE AS MEMORY COST HAS GONE DOWN.

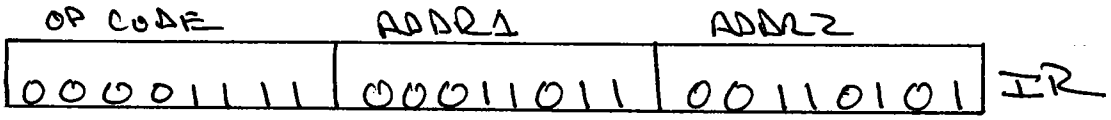
<u>EX</u>

SUPPOSE OUR MACHINE LANGUAGE INSTRUCTIONS CONSIST OF AN 8 BIT OP CODE FOLLOWED BY TWO 8 BIT ADDRESS FIELDS. (i.e. AT MOST 256 OP CODES, AND 256 BYTES IN MEMORY.)

SUPPOSE WE WISH TO MOVE THE CONTENTS OF CELL 27 TO CELL 53, AND THAT THE OP-CODE FOR THIS OPERATION IS 15.

15 = 1111, 27 = 11011, 53 = 110101.

THE BIT STRING FOR THIS INSTRUCTION IS THEN:



IN THE SEQUEL WE WILL NOT EXPRESS SUCH INSTRUCTIONS IN BINARY AS ABOVE. INSTEAD WE WILL USE SHORTHAND NOTATION LIKE:

MOVE 27, 53

WE MUST KEEP IN MIND THOUGH THAT THIS SHORTHAND STANDS FOR THE FULL BINARY INSTRUCTION.

CONVENTIONS

WE WILL USE CAPITOLS X, Y, Z FOR CELL ADDRESSES, AND LOWER CASE a, b, c FOR VALUES STORED IN CELLS. CON(X) MEANS THE CONTENTS OF THE CELL WITH ADDRESS X. ASSUME OUR ALU CONTAINS JUST ONE REGISTER: R.

MACHINE LANGUAGE INSTRUCTIONS CAN BE GROUPED INTO FOUR CLASSES: