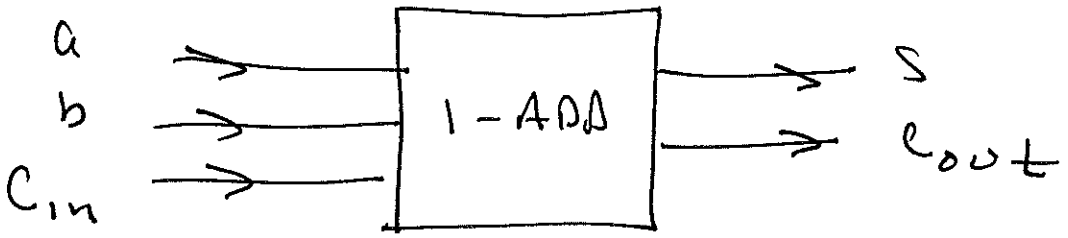
CMPS 10 11-17-09

Recall: Goal to Design

n-bit full adder

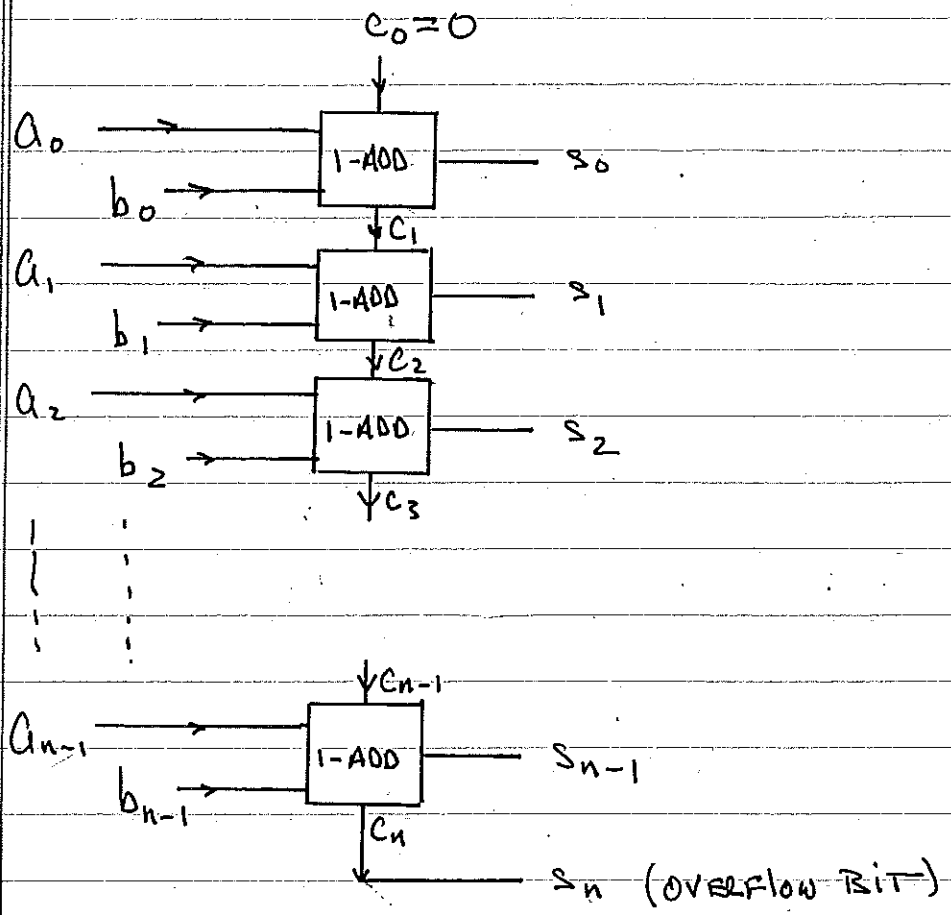
- 1ST Design 1-bit adder



- 2ND Assemble n 1-adder circuits to build an n-bit adder.

TO CONSTRUCT THE FULL n-BIT ADDER WE COMBINE n COPIES OF THE ABOVE CIRCUIT.

$$\underbrace{[a_{n-1}\cdots a_0]_2 + [b_{n-1}\cdots b_0]_2}_{\text{INPUTS}} = \underbrace{[s_n s_{n-1}\cdots s_0]_2}_{\text{OUTPUT}}$$



THE n-BIT FULL ADDER USES $47n$ TRANSISTORS. FOR EXAMPLE, A 32-BIT ADDER USES $47 \cdot 32 = 1504$ TRANSISTORS

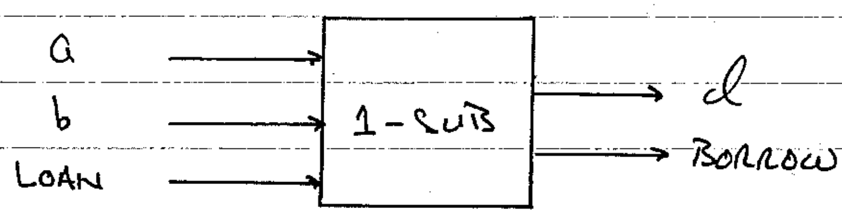
WHAT ABOUT SUBTRACTION?

EX

```
  0 10 1
  X  X 0 1 = 13
  0  1 1 1 = 7
  ----------
  0  1 1 0 = 6
```

EXCERCISE

DESIGN A 1-BIT SUBTRACTION CIRCUIT

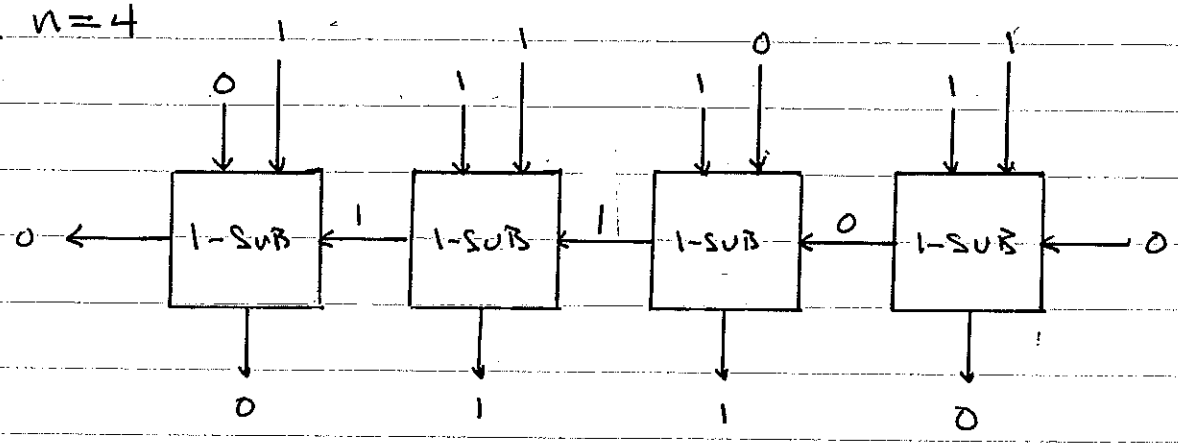


IF $a - b - \text{LOAN} < 0$ THEN BORROW = 1, OTHERWISE BORROW = 0. THEN $d = 2\,\text{BORROW} + a - b - \text{LOAN}$

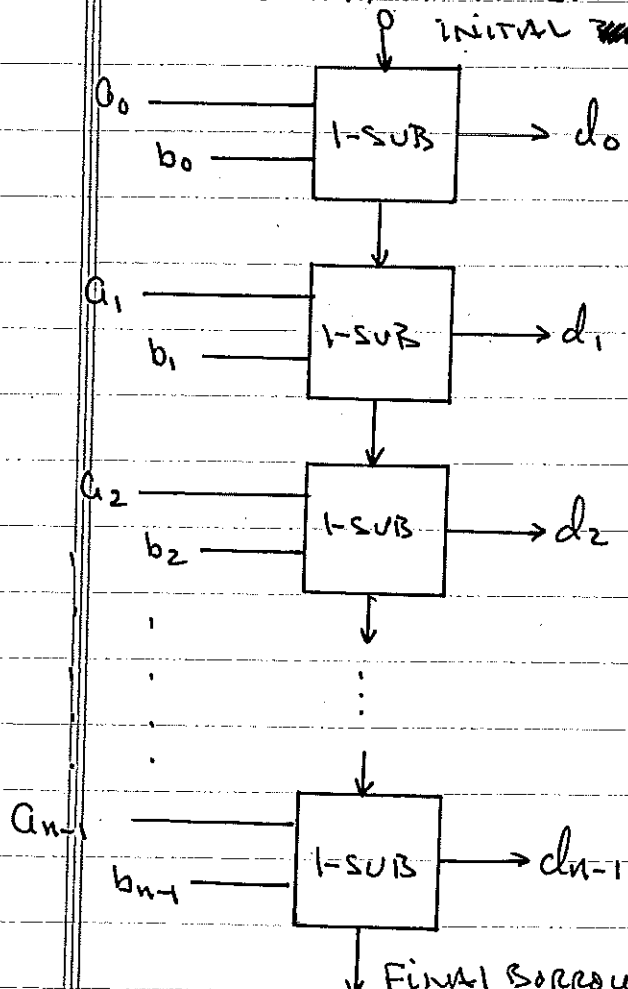
a	b	LOAN	d	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

USING 1-SUB WE CAN BUILD AN n-BIT SUBTRACTOR

EX $n=4$



THE GENERAL n-BIT SUBTRACTOR LOOKS LIKE

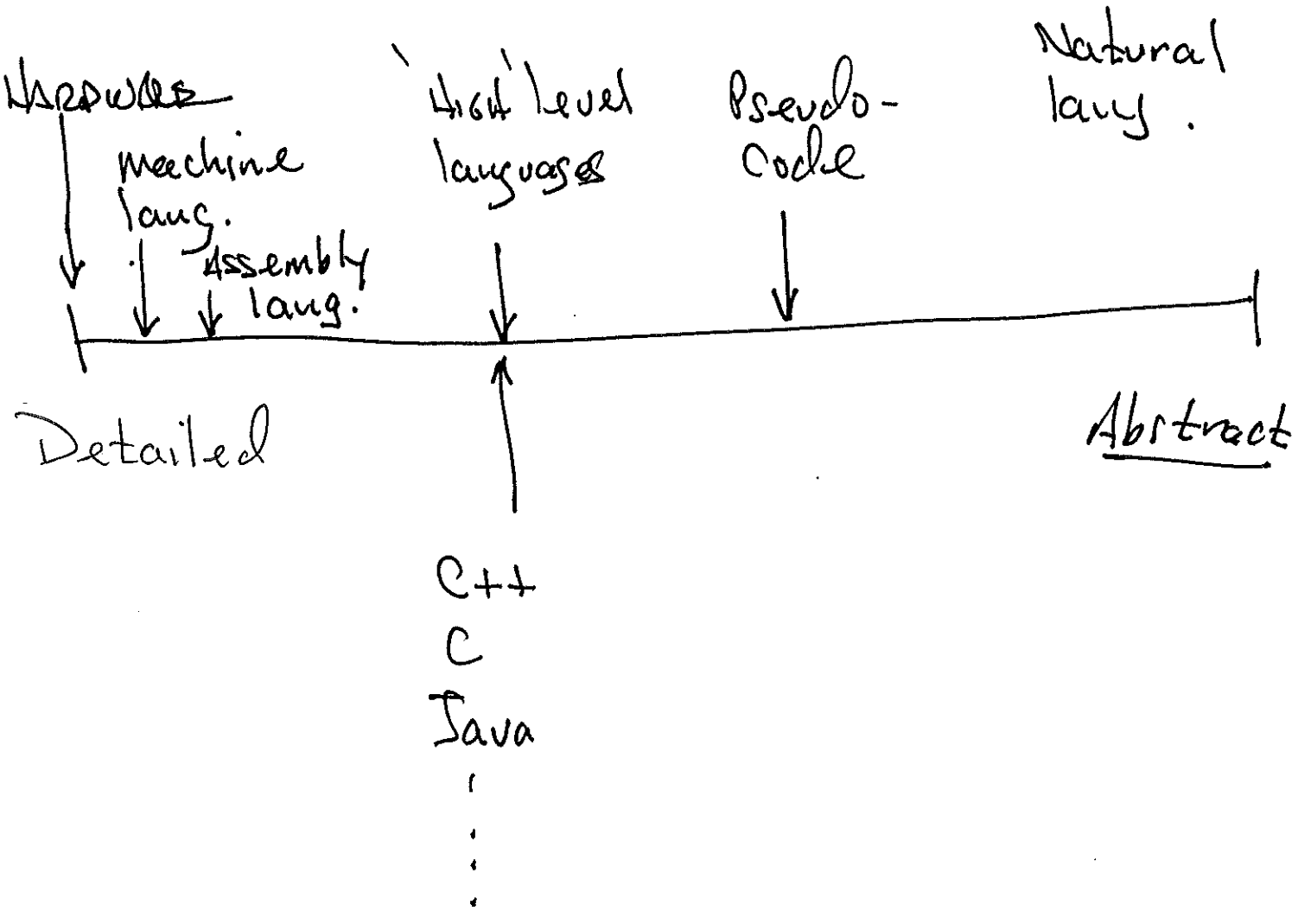


$$[d_0 \cdots d_{n-1}] = [a_0 \cdots a_{n-1}] - [b_0 \cdots b_{n-1}]$$

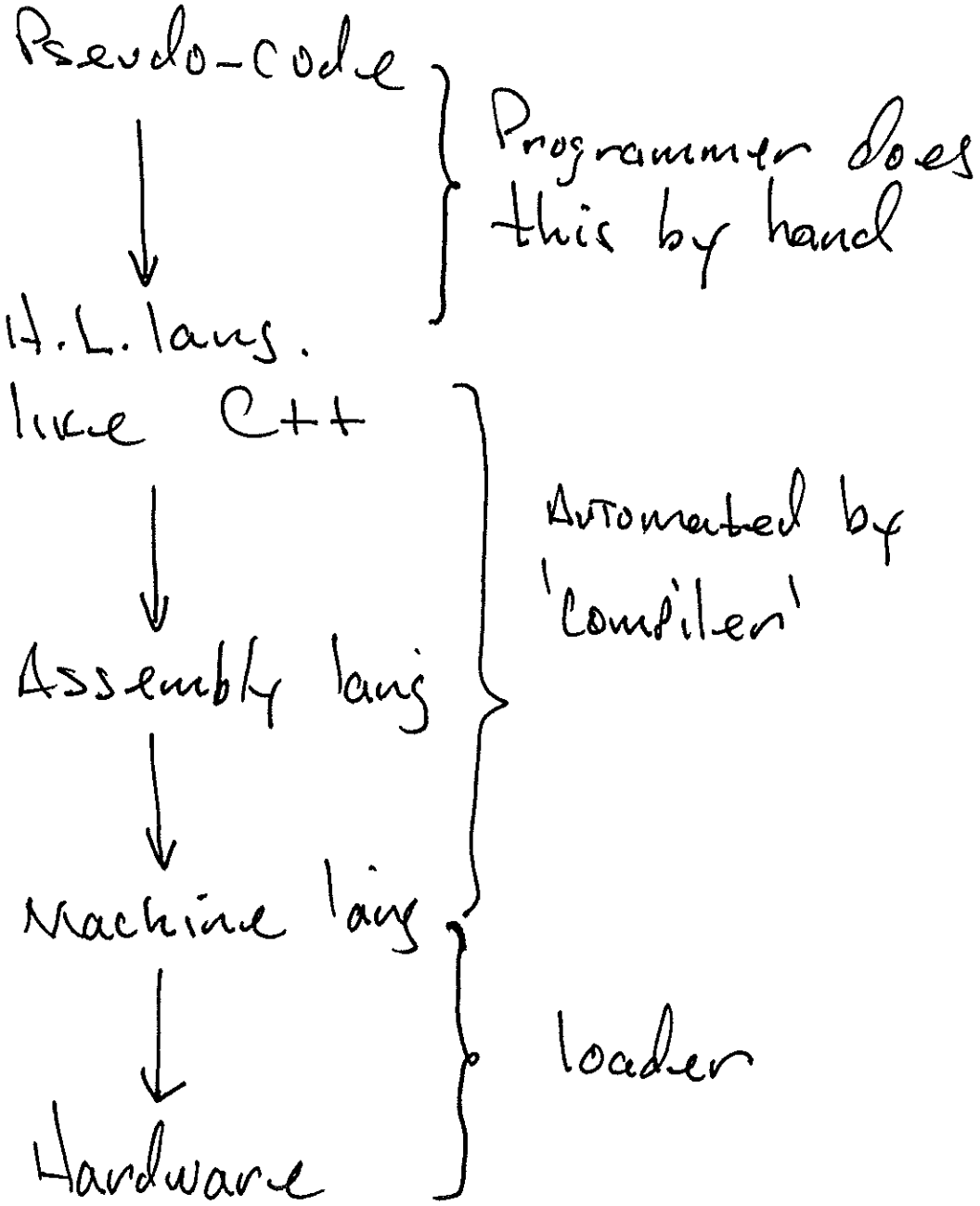
$$\text{COMPARISON BIT} = \begin{cases} 1 & \text{IF } [a_0 \cdots a_{n-1}] < [b_0 \cdots b_{n-1}] \\ 0 & \text{OTHERWISE} \end{cases}$$

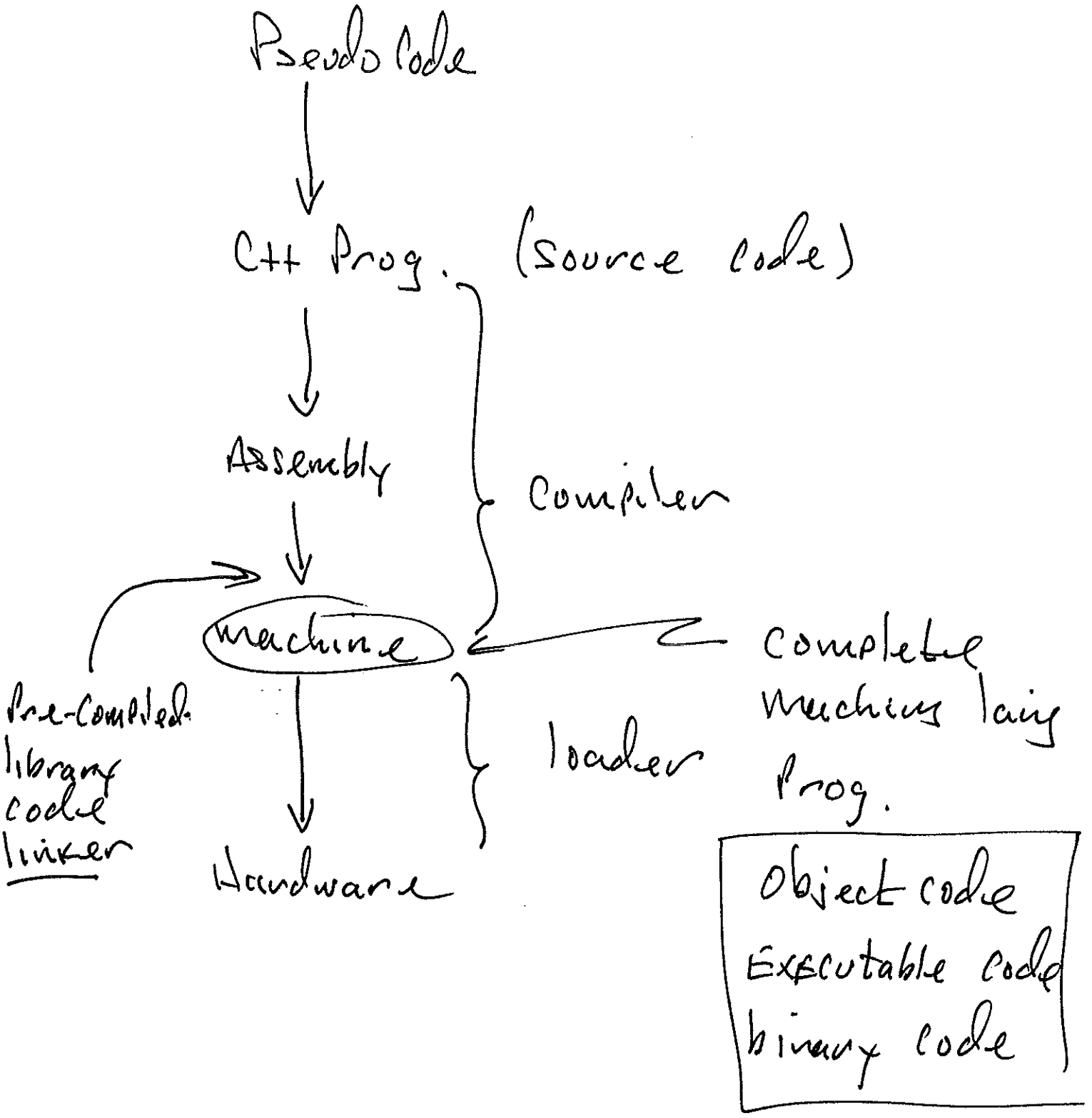
Higher level languages

Abstractness Continuum



TRANSLATION Process




Pseudo code
C++ Prog. (Source code)
Assembly
Compiler
machine
Pre-Compiled library code
linker
Hardware
loader
complete machine lang Prog.
Object code
Executable code
binary code