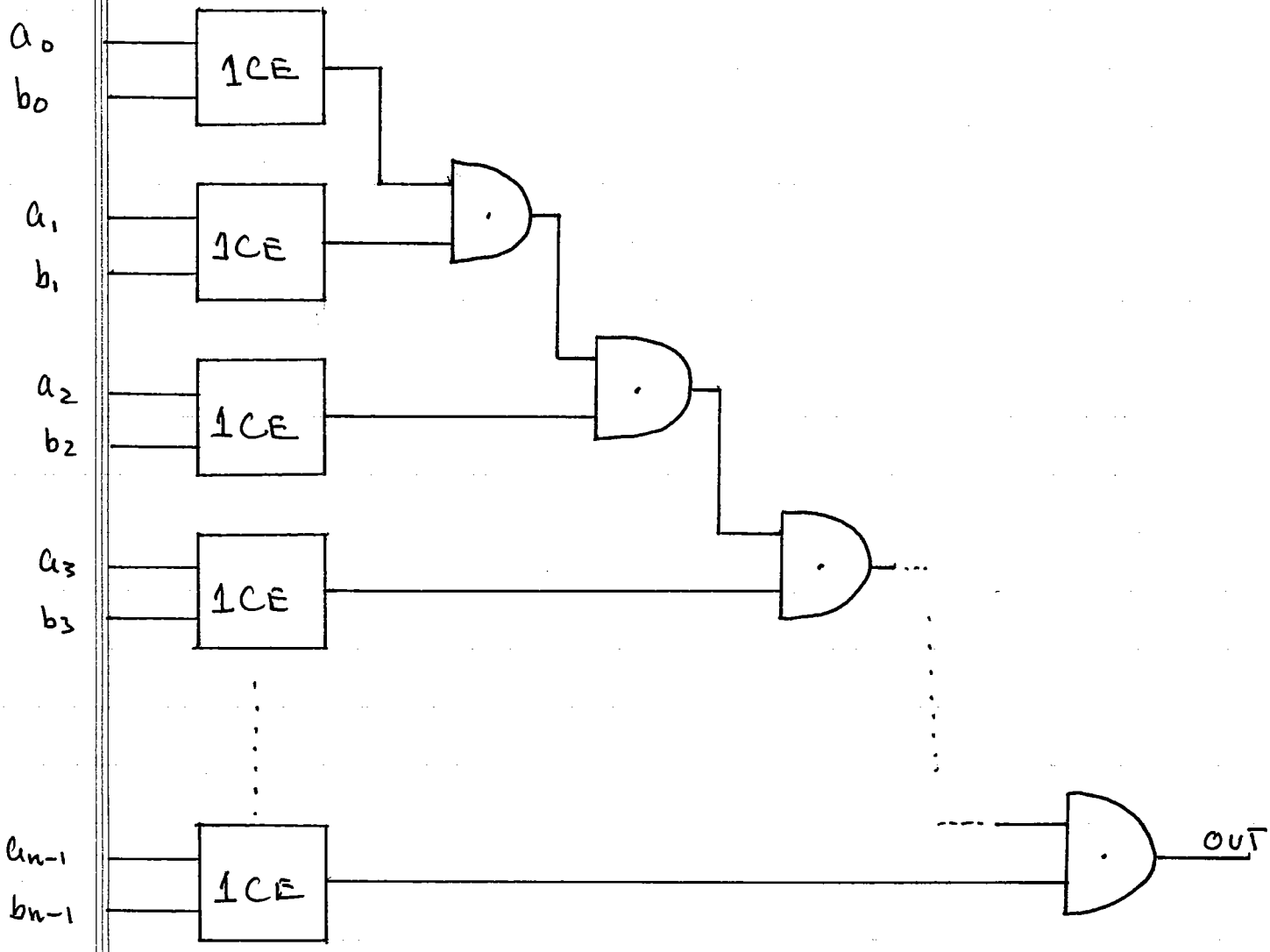
INPUTS: TWO n BIT BINARY NUMBERS
$[a_{n-1} \cdots a_0]_2$, $[b_{n-1} \ldots b_0]_2$

OUTPUT: 1 IF EACH $a_i = b_i$ $(0 \le i \le n-1)$,
0 OTHERWISE



HOW MANY ROWS AND COLUMNS WOULD THE TRUTH TABLE FOR THIS CIRCUIT HAVE ?

ANSWER: 2^{2n} ROWS
$2n+1$ COLUMNS

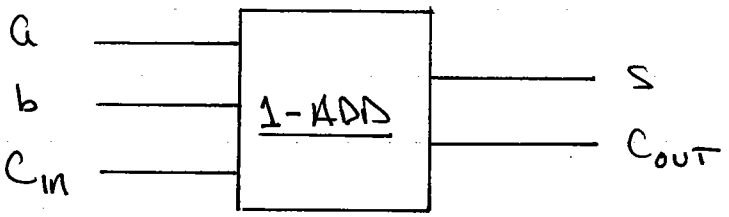
HOW MANY TRANSISTORS ARE NEEDED TO BUILD THIS CIRCUIT? ANSWER: $10n - 2$

OUR NEXT TASK IS TO CONSTRUCT A CIRCUIT WHICH ADDS TWO n BIT BINARY NUMBERS. THIS CIRCUIT IS CALLED AN n-BIT FULL ADDER.

EX.

$$\begin{array}{r} 1\,0\,1\,1\,0\,1\,0\,0 \\ 1\,0\,0\,1\,0\,1\,1\,0 \\ \hline 1\,0\,1\,1\,0\,0\,1\,1 \\ \hline 1\,0\,1\,0\,0\,1\,0\,0\,1 \end{array} \qquad n=8$$

WE START BY BUILDING A 1-BIT ADDER WHICH TAKES THREE INPUTS (TWO BITS AND A CARRY) AND RETURNS TWO OUTPUTS (SUM AND NEW CARRY)



THESE 1-BIT ADDERS CAN THEN BE COMBINED TO FORM A PHYSICAL IMPLEMENTATION OF THE ABOVE ALGORITHM (WHICH IS ESSENTIALLY THE ADDITION ALGORITHM GIVEN ON THE FIRST DAY OF CLASS.)

THE TRUTH TABLE FOR 1-ADD IS:

INPUTS			OUTPUTS	
a	b	c	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

THE GENERAL PROCEDURE FOR CONSTRUCTING A CIRCUIT IS AS FOLLOWS:

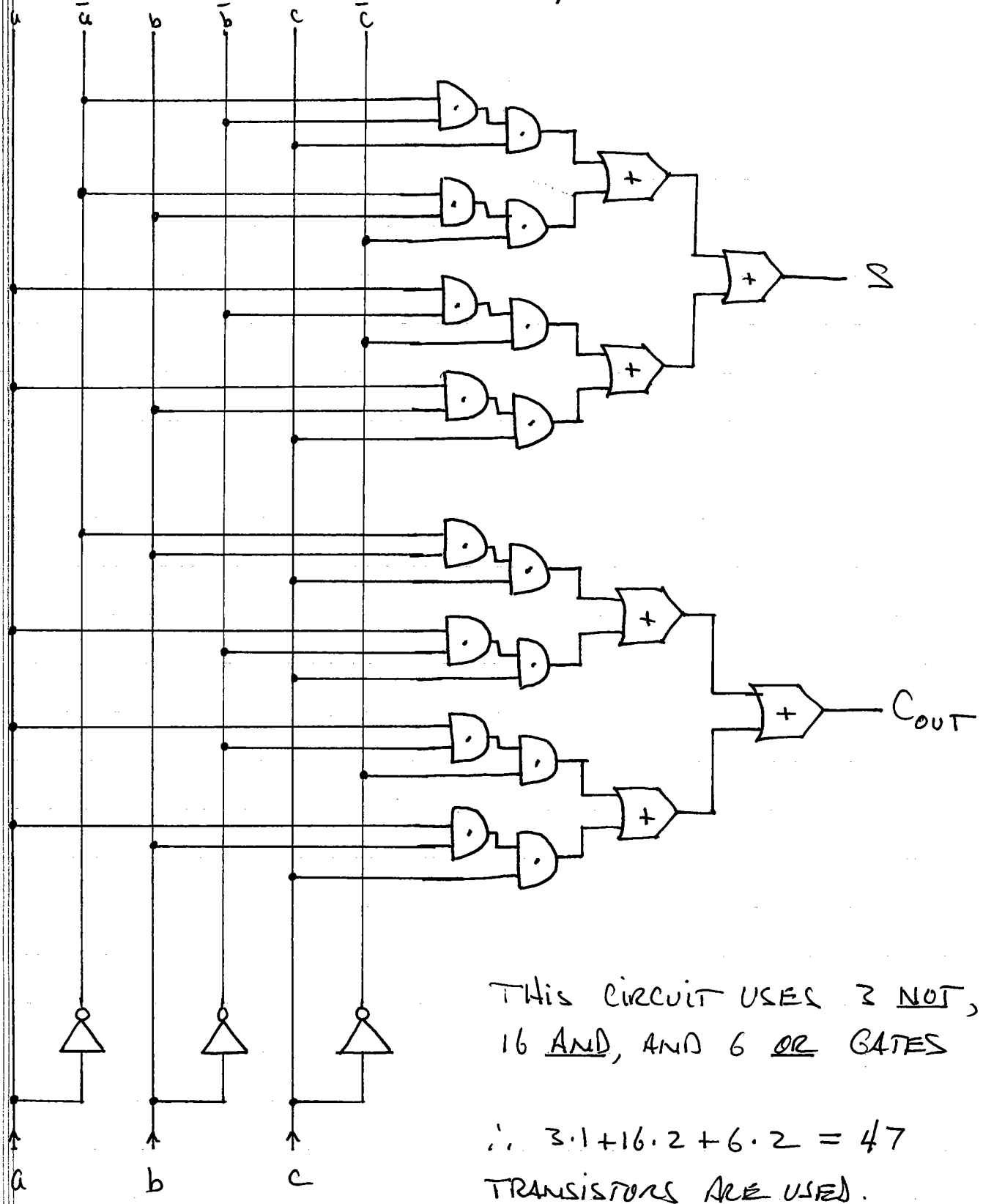
1.) FOR EACH OUTPUT COLUMN
2.) FOR EACH ROW CONTAINING A 1 IN THAT COLUMN
3.) FORM "PRODUCT" CORRESPONDING TO INPUTS
4.) FORM THE "SUM" OF THESE "PRODUCTS"
5.) DESIGN A CIRCUIT CORRESPONDING TO THE RESULTING SET OF LOGICAL EXPRESSIONS.

FROM THE ABOVE TABLE WE GET:

$$C_{OUT} \equiv (\bar{a} \cdot b \cdot c) + (a \cdot \bar{b} \cdot c) + (a \cdot b \cdot \bar{c}) + (a \cdot b \cdot c)$$

$$S \equiv (\bar{a} \cdot \bar{b} \cdot c) + (\bar{a} \cdot b \cdot \bar{c}) + (a \cdot \bar{b} \cdot \bar{c}) + (a \cdot b \cdot c)$$

WE NEED A SYSTEMATIC WAY TO DRAW CIRCUITS:



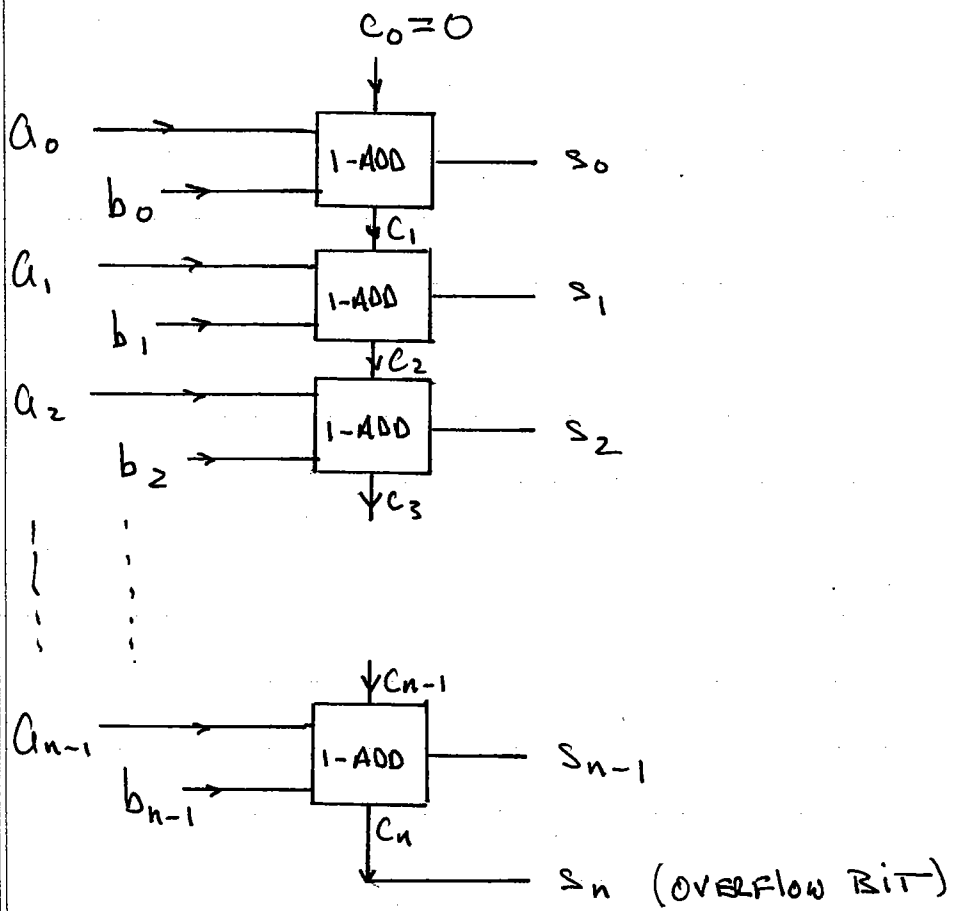
THIS CIRCUIT USES 3 NOT, 16 AND, AND 6 OR GATES

$\therefore 3 \cdot 1 + 16 \cdot 2 + 6 \cdot 2 = 47$

TRANSISTORS ARE USED.

TO CONSTRUCT THE FULL n-BIT ADDER WE COMBINE n COPIES OF THE ABOVE CIRCUIT.

$$\underbrace{[a_{n-1}\cdots a_0]_2 + [b_{n-1}\cdots b_0]}_{\text{INPUTS}} = \underbrace{[s_n s_{n-1}\cdots s_0]_2}_{\text{OUTPUT}}$$



THE n-BIT FULL ADDER USES $47n$ TRANSISTORS. FOR EXAMPLE, A 32-BIT ADDER USES $47 \cdot 32 = 1504$ TRANSISTORS

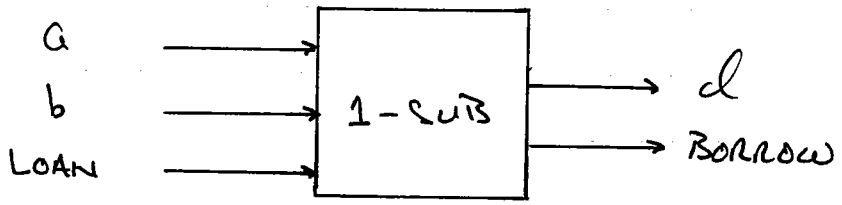
WHAT ABOUT SUBTRACTION ?

EX

$$\begin{array}{r} {}^{0}{}^{10} \\ \not{1}\not{0}1 \\ 0111 \\ \hline 0110 \end{array} \quad \begin{array}{l} = 13 \\ = 7 \\ \\ = 6 \end{array}$$

EXCERCISE

DESIGN A 1-BIT SUBTRACTION CIRCUIT

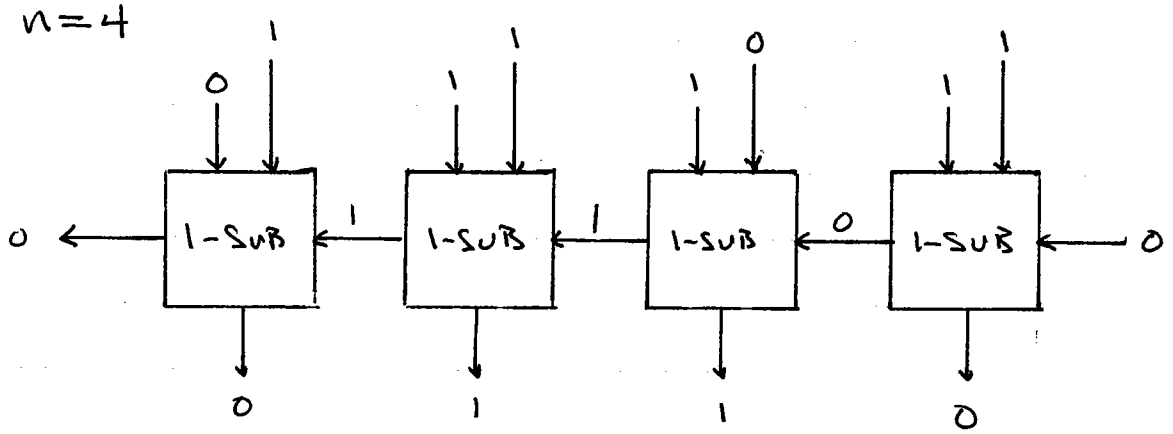


IF $a-b-LOAN < 0$ THEN BORROW = 1, OTHERWISE BORROW = 0. THEN $d = 2 \cdot BORROW + a - b - LOAN$

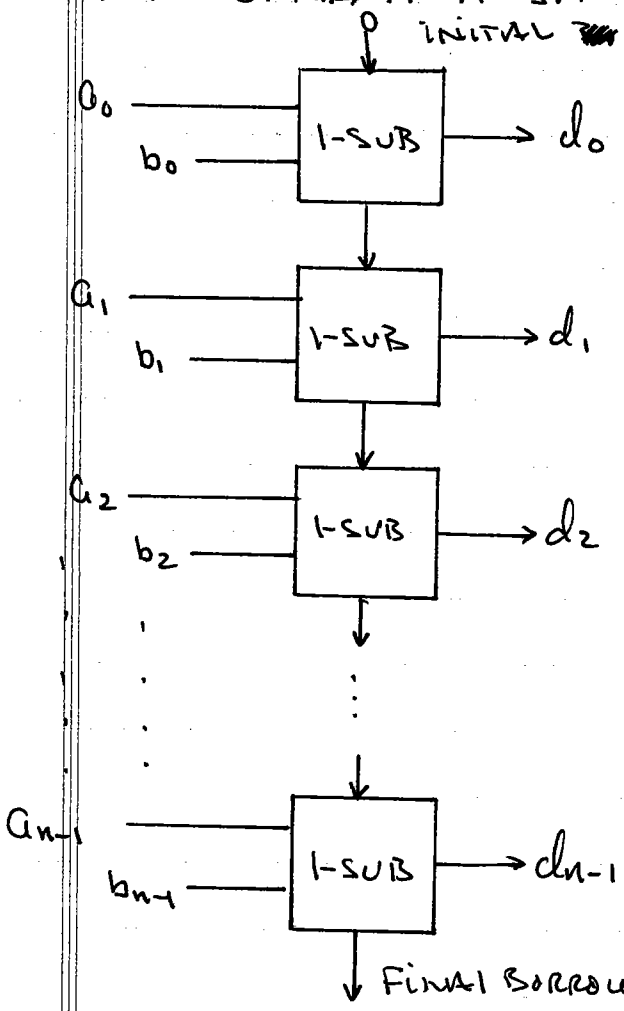
a	b	LOAN	d	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

USING 1-SUB WE CAN BUILD AN n-BIT SUBTRACTOR

EX $n=4$



THE GENERAL n-BIT SUBTRACTOR LOOKS LIKE



$$[d_0 \cdots d_{n-1}] = [a_0 \cdots a_{n-1}] - [b_0 \cdots b_{n-1}]$$

$$\text{COMPARISON BIT} = \begin{cases} 1 & \text{IF } [a_0 \cdots a_{n-1}] < [b_0 \cdots b_{n-1}] \\ 0 & \text{OTHERWISE} \end{cases}$$