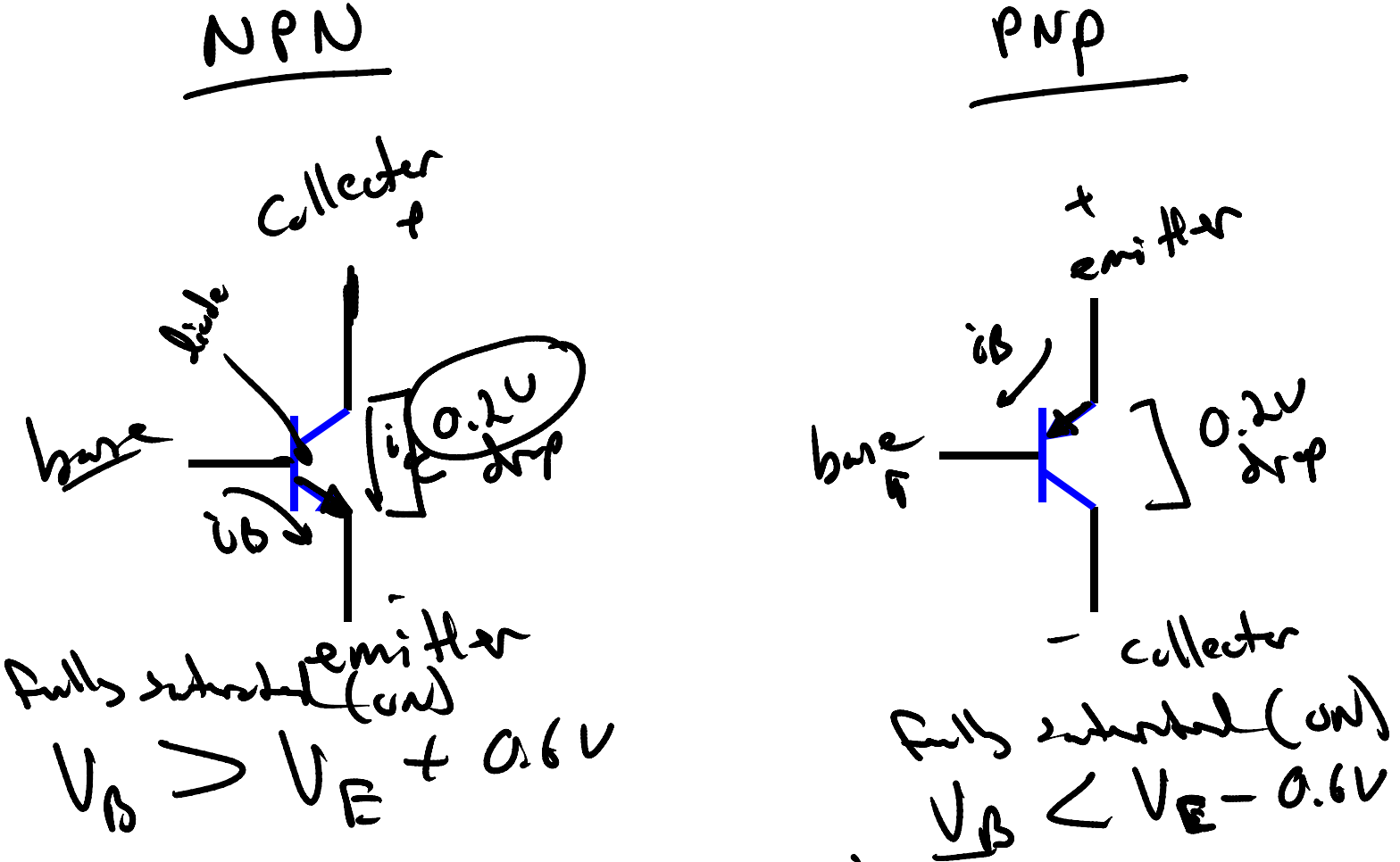
- digital input outputs
- power behavior
- pullup transistors

Digital I/O

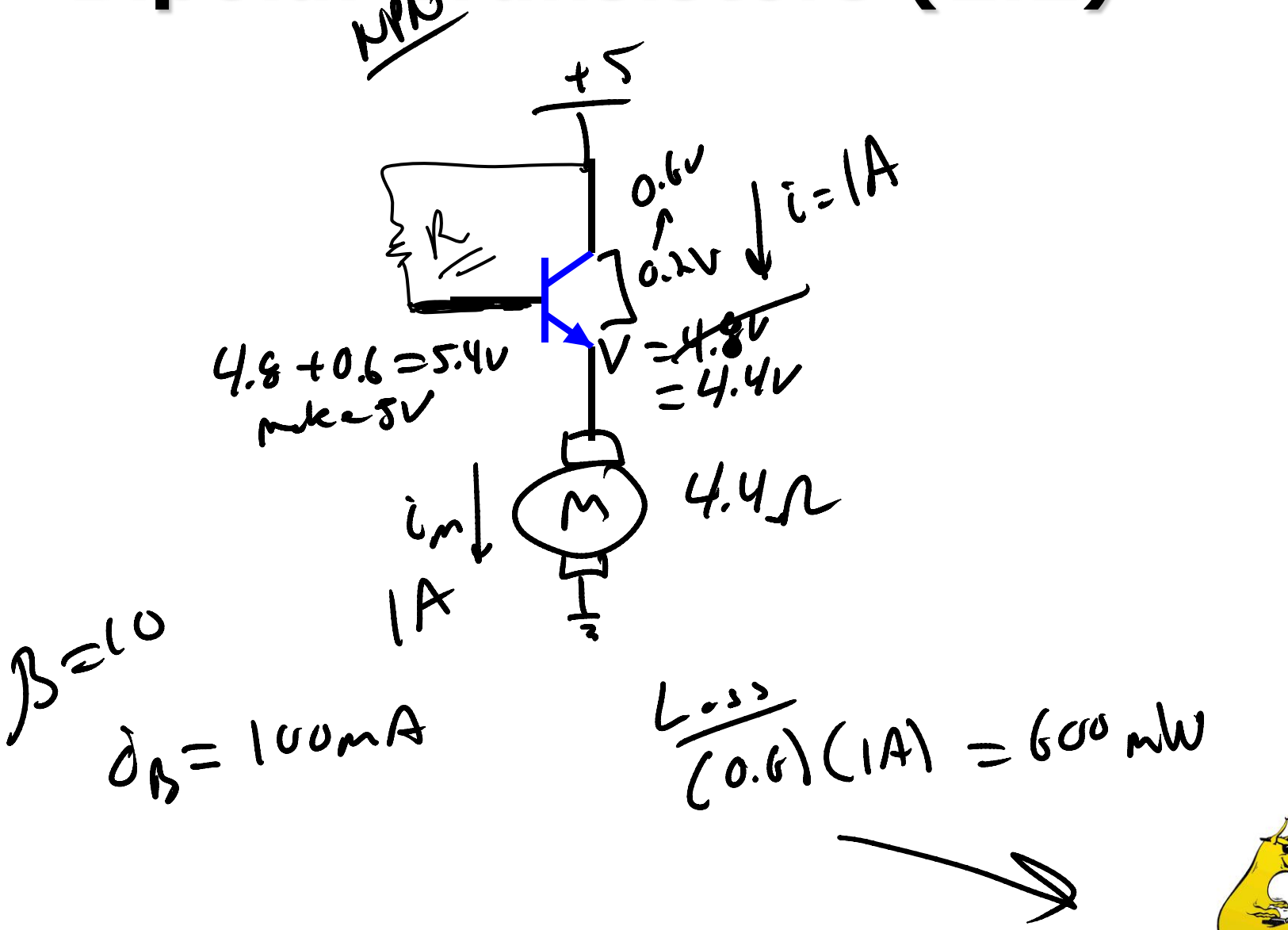
Cyrus Bazeghi

Winter 2010

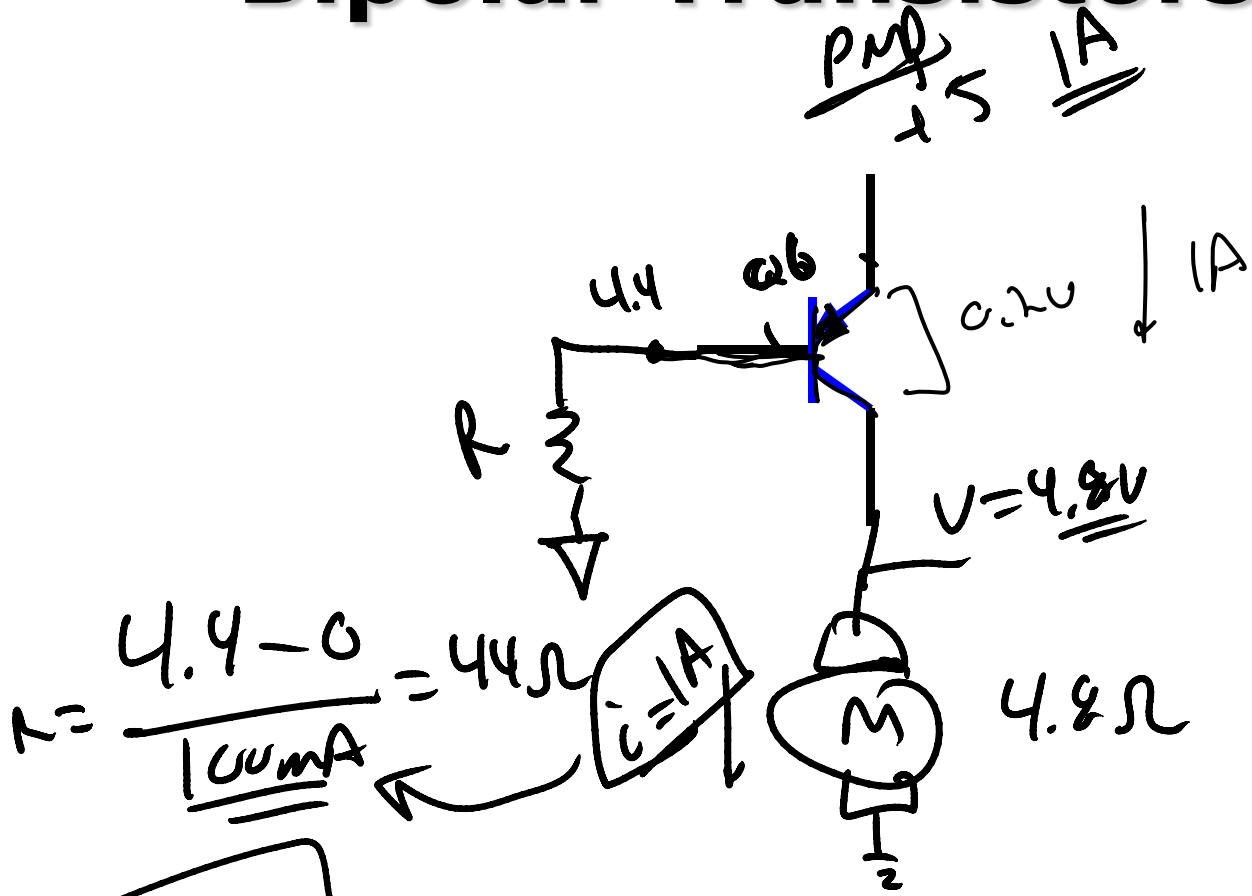
Bipolar Transistors (1.2)



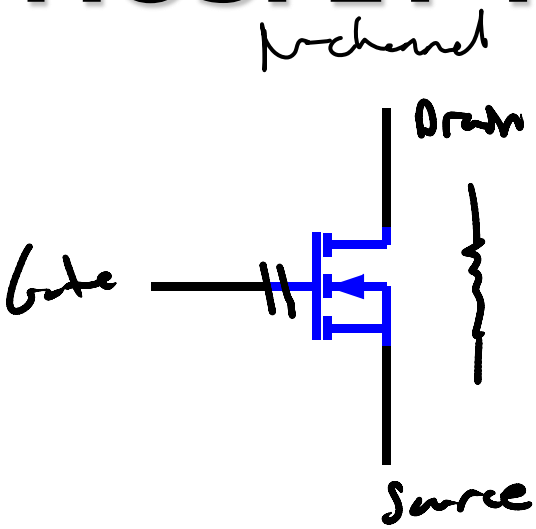
Bipolar Transistors (2.2)

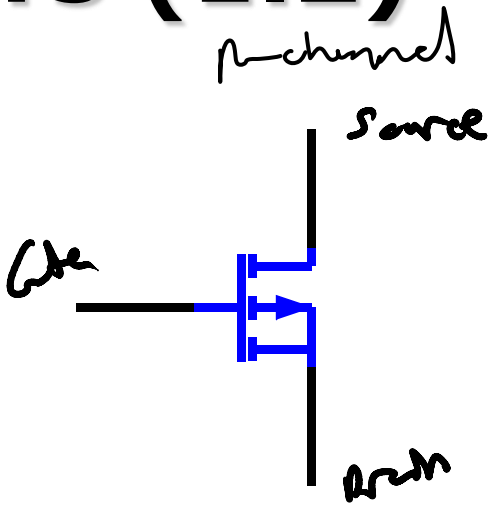


Bipolar Transistors (2.2)



MOSFET Transistors (1.2)





$V_G > V_{source} + threshold$

10 V - power mosFET

2-4 V - logic levels

$R_{DS_{ON}} = 2\text{-}3\ m\Omega$

"analog switches"

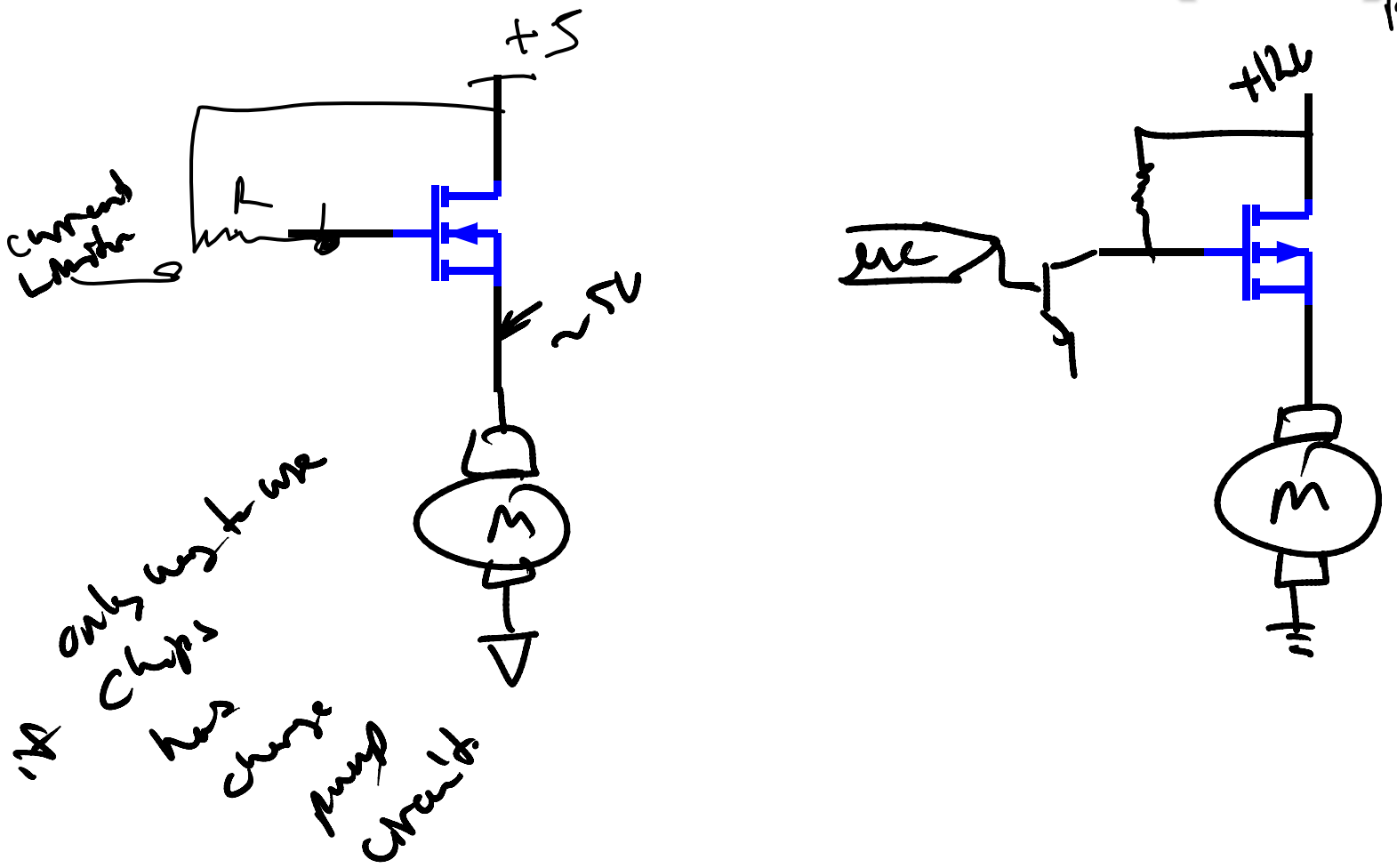
~100 V 30 A

$V_G < V_S - threshold$

3-4 x price

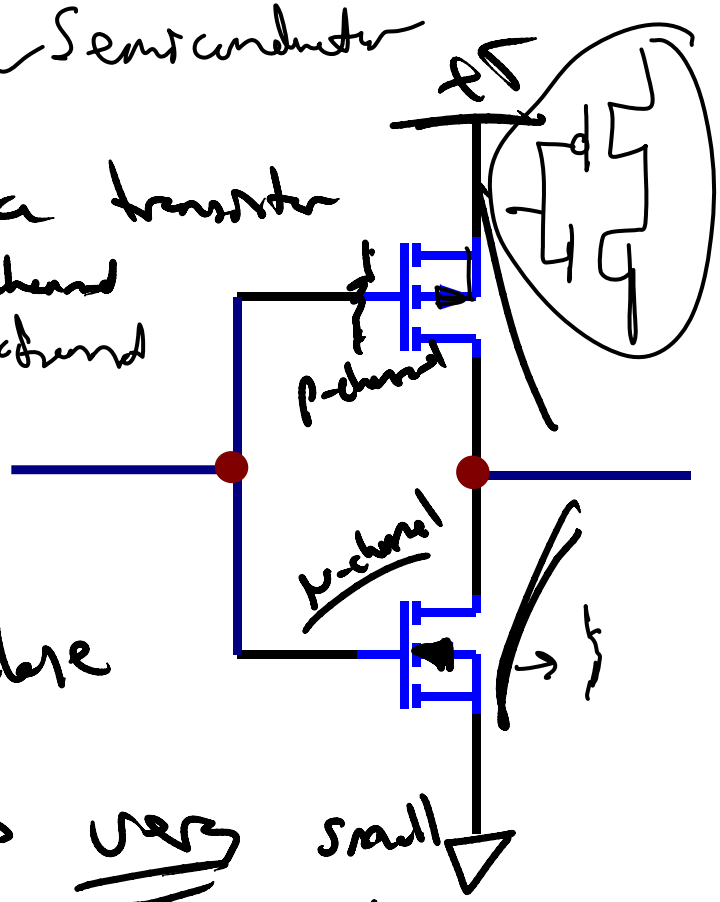
~2-3 x $R_{DS_{ON}}$

MOSFET Transistors (2.2)



What is CMOS?

- Complementary Metal Oxide Semiconductor
- Every place you need a transistor you use two FETs (p-channel, n-channel) in pairs.



Nice advantages

Can get outputs very close to supply & gnd.

Since resistance is very small within mV's of the rails

Digital Inputs

What are the Voltage Levels?

TTL – trans. trans Logic

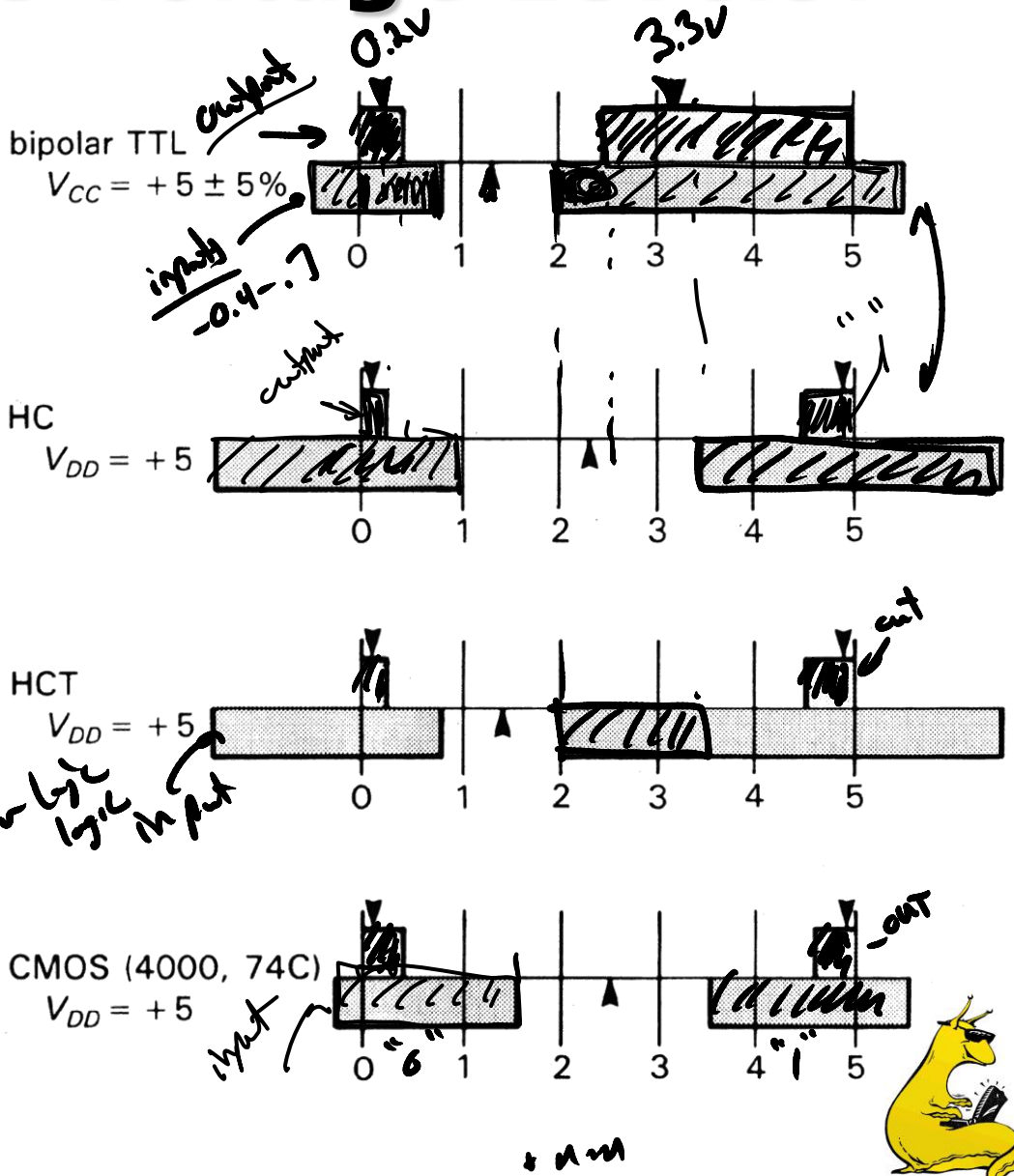
HC – high speed CMOS

HCT – w/ TTL inputs

Old family CMOS – slower

older RTL – resistor transistor logic

DTL – diode

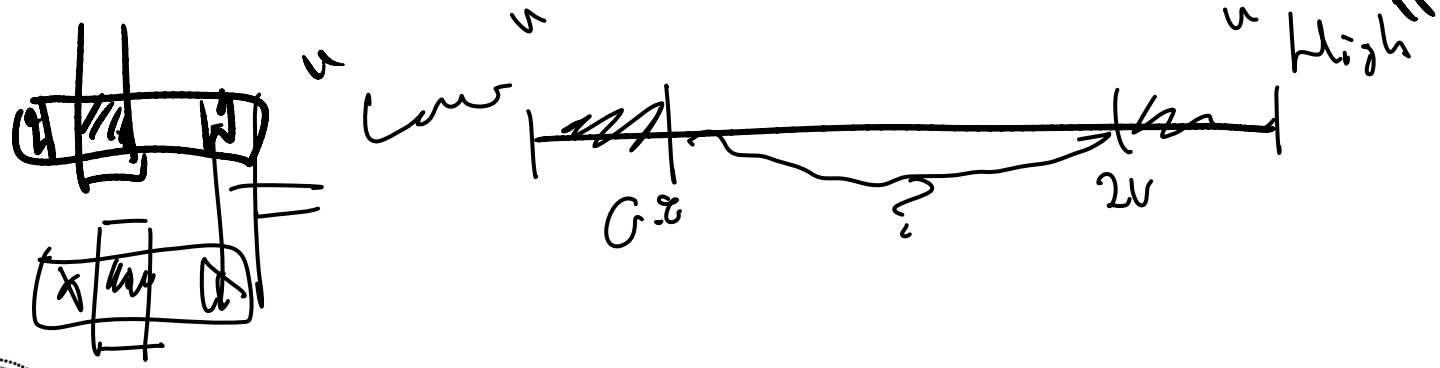


How is the Voltage Specified?

TTL NAND Gate

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			-0.4			-0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	-55		125	0		70	°C



It takes Voltage and Current to make a device work!

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

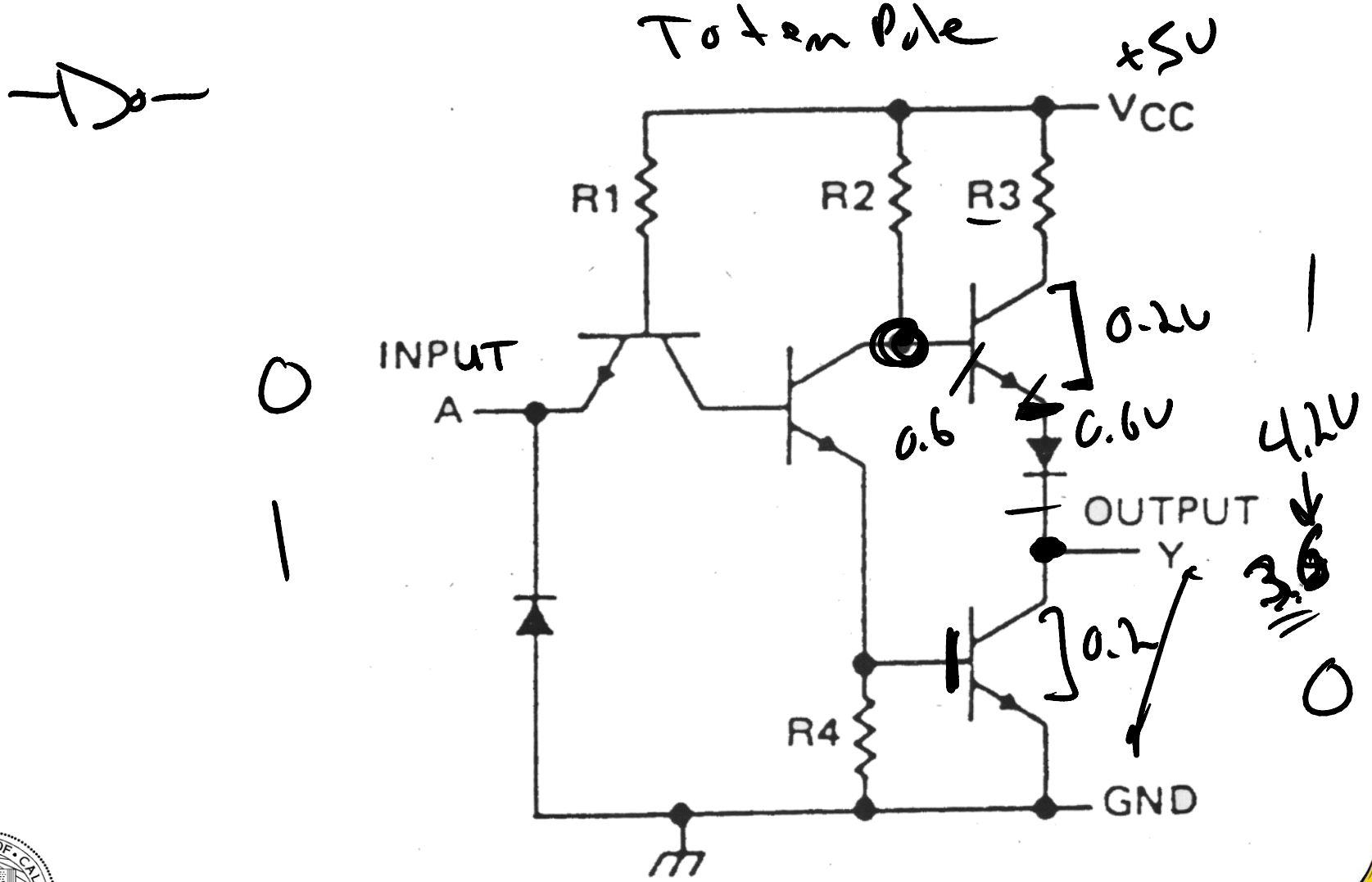
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = -18 mA				-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				-0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	-20		-100	mA
			DM74	-20		-100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Interconnecting

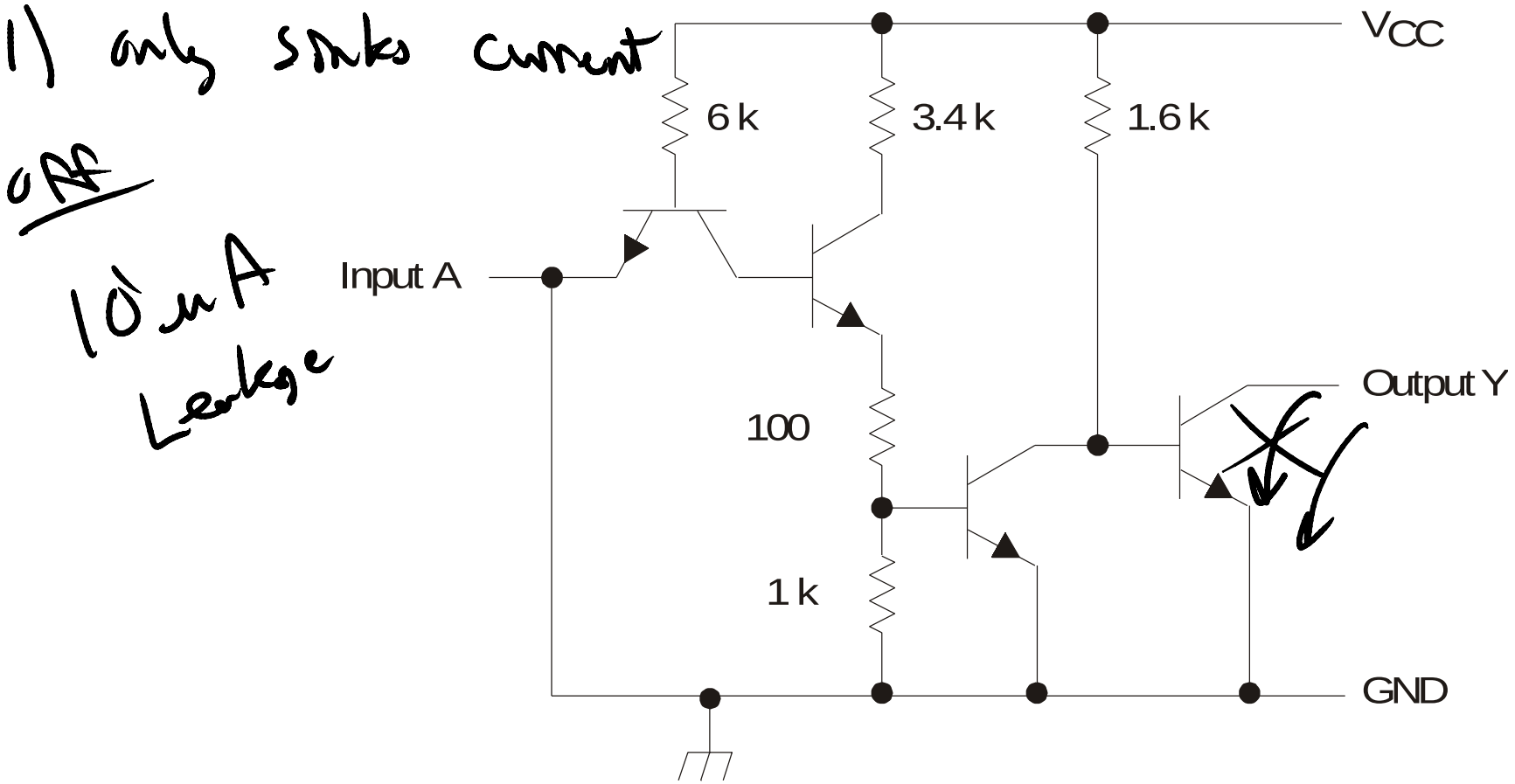
TO → / FROM ↓	TTL	HCT ACT	HC AC	HC, AC @3.3V	NMOS LSI	4000B, 74C @5V	4000B, 74C @10V
TTL	OK	OK	A	OK	OK	A	B
HCT ACT	OK	OK	OK	NO	OK	OK	B
HC AC	OK	OK	OK	NO	OK	OK	B
HC, AC @3.3V	OK	OK	NO	OK	OK	B	B
NMOS LSI	OK	OK	A	OK	OK	A	B
4000B, 74C @5V	OK[a]	OK	OK	NO	OK	OK	B
4000B, 74C @10V	C	C	C	C	C	C	OK

[a] with limited fanout. A – pullup to +5V, or use HCT as interface.
B – use *i)* OC pullup to +10V, or *ii)* 40109, 14504, or LTC1045 level translator.
C – use 74C901/2, 4049/50, 14504, or LTC1045 level translator.

Digital Logic: Bipolar TTL Output

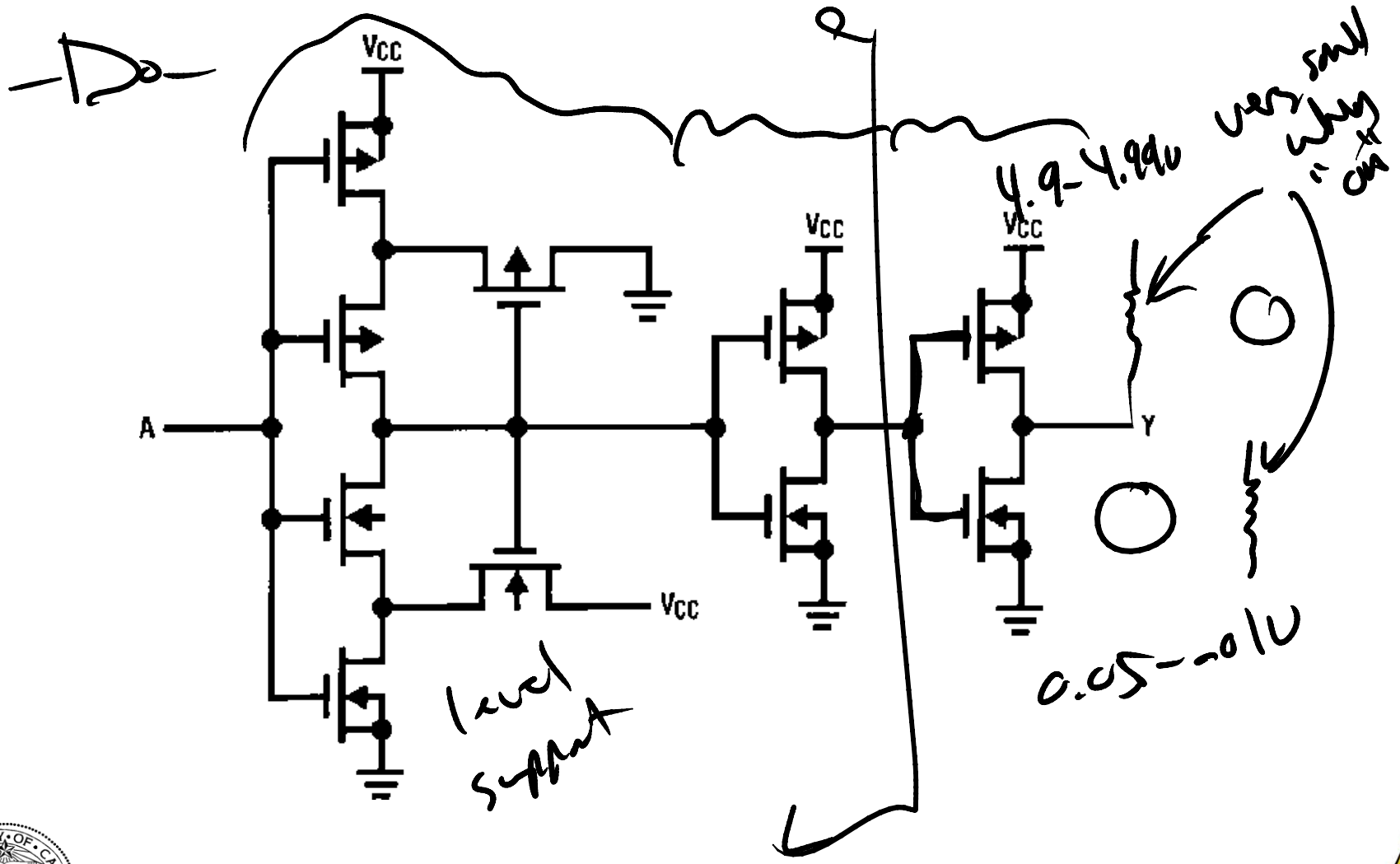


Digital Logic: Open Collector Output

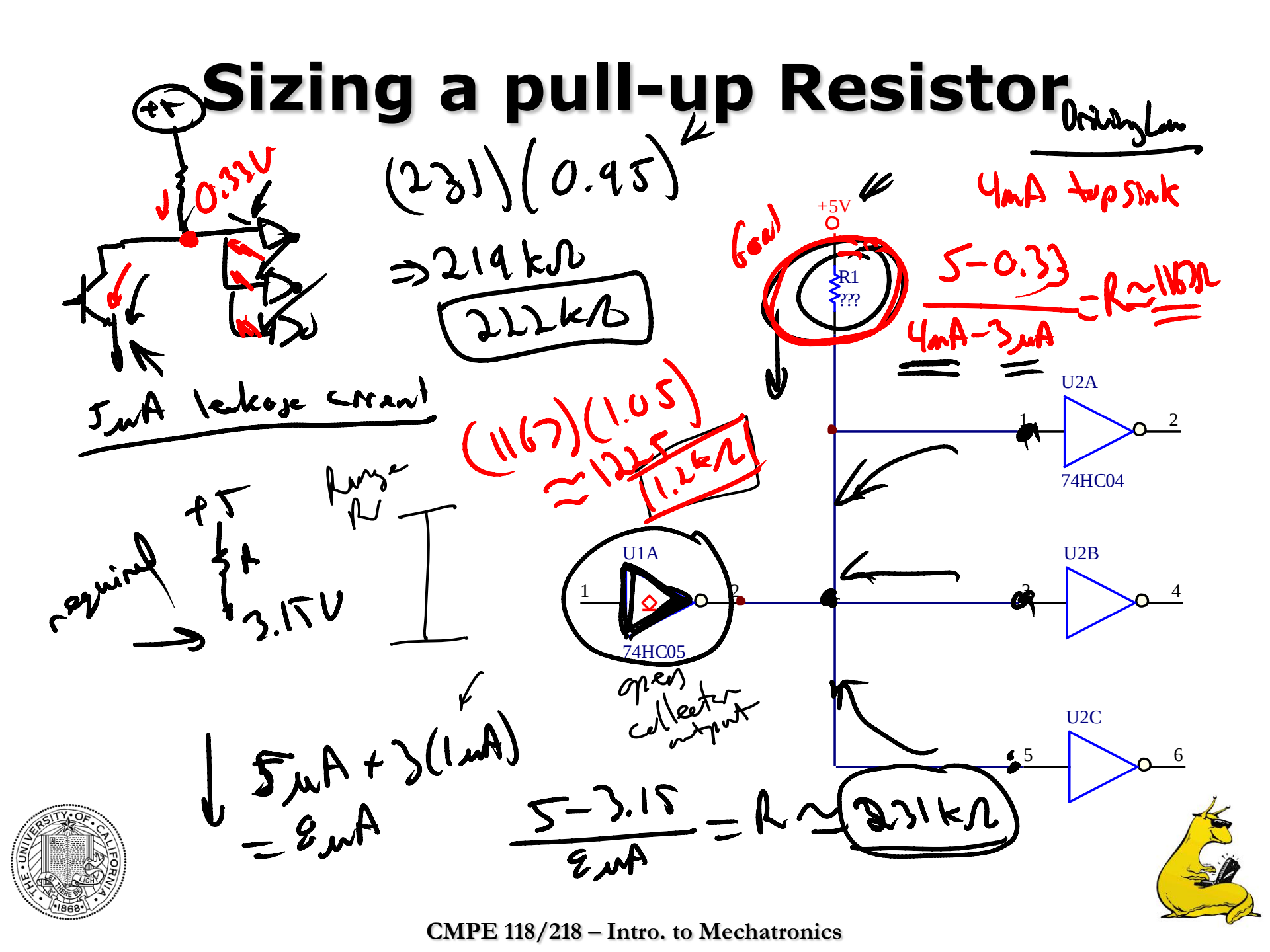


Resistor values shown are nominal.

Digital Logic: CMOS Totem Pole



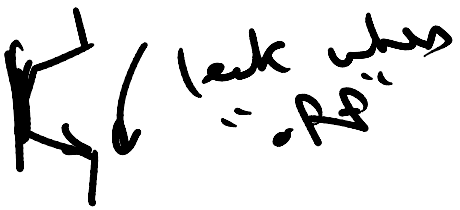
Sizing a pull-up Resistor



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL},	$V_O = V_{CC}$	6 V		0.01	0.5		10		5	μA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

$I_{OH} = 5\mu A$



74HC04

$V_{IH} = 3.15V$ @ 1mA

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		2.0	20	40	μA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$		6 V		0.01	0.5		10		5	μA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = –40 to 85°C	T_A = –55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IL}$						
		$\|I_{OUT}\| \le 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IL}$						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$						
		$\|I_{OUT}\| \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Absolute Maximum Ratings

CD54HC00, CD54HCT00, CD74HC00, CD74HCT00

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} ..... -0.5V to 7V
DC Input Diode Current, I_{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ 20mA
DC Output Diode Current, I_{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ 20mA
DC Output Source or Sink Current per Output Pin, I_O
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ 25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} 50mA

Operating Conditions

Temperature Range (T_A) ..... -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types ..... 2V to 6V
HCT Types ..... 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O ..... 0V to V_{CC}
Input Rise and Fall Time
2V ..... 1000ns (Max)
4.5V ..... 500ns (Max)
6V ..... 400ns (Max)

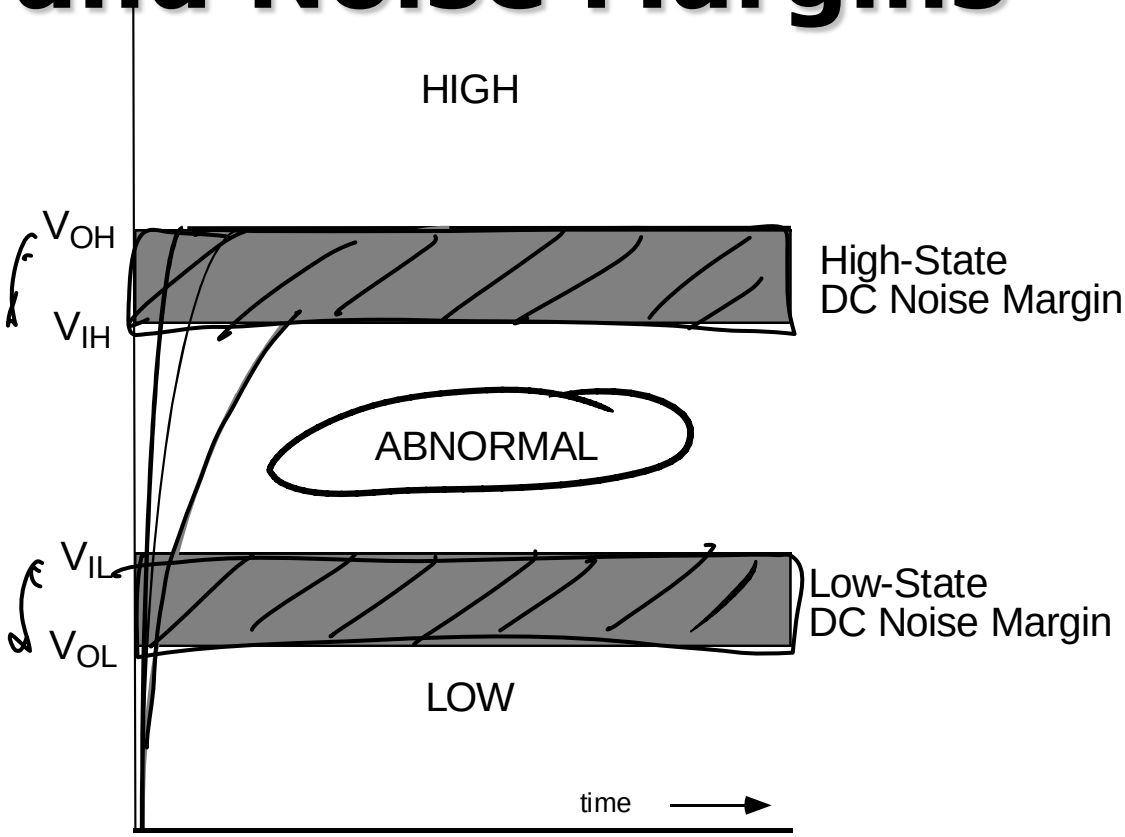
Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
PDIP Package 80
SOIC Package 86
Maximum Junction Temperature (Hermetic Package or Die) ... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not i

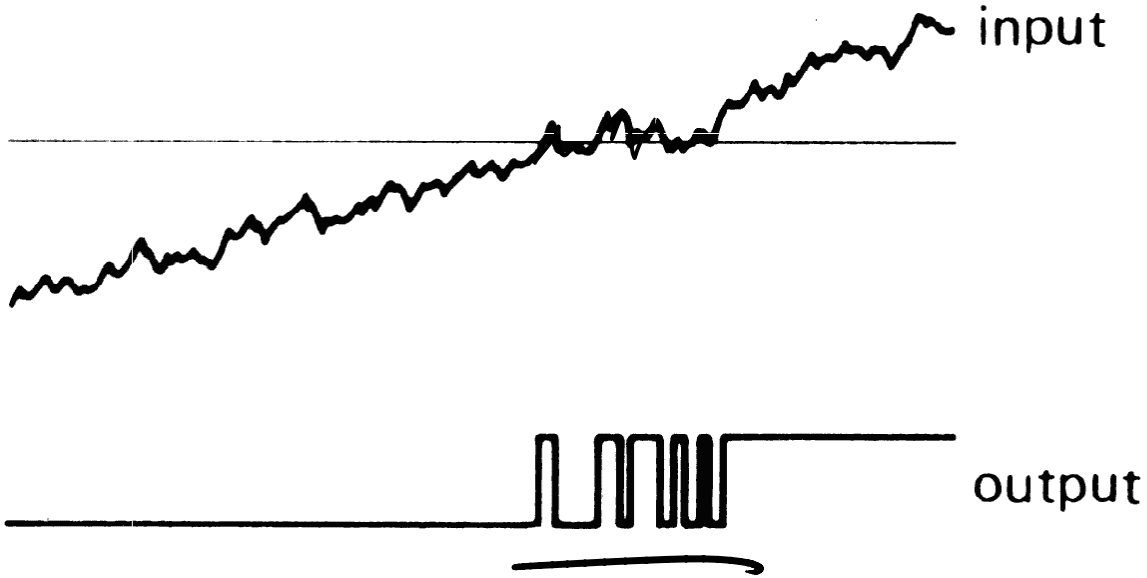
Logic Levels and Noise Margins

specs
min/max
rise + fall
time



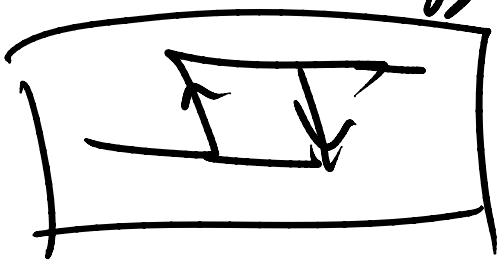
For TTL	For CMOS @V_{CC}=5V
V_{OL}=0.4V	V_{OL}=0.5V
V_{IL}=0.8V	V_{IL}=1.5V
V_{IH}=2.0V	V_{IH}=3.5V
V_{OH}=2.4V	V_{OH}=4.5V

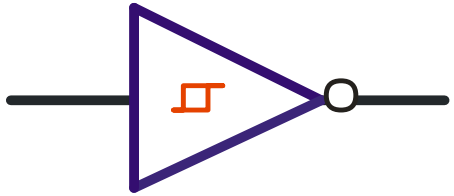
What about Slowly Changing Inputs?



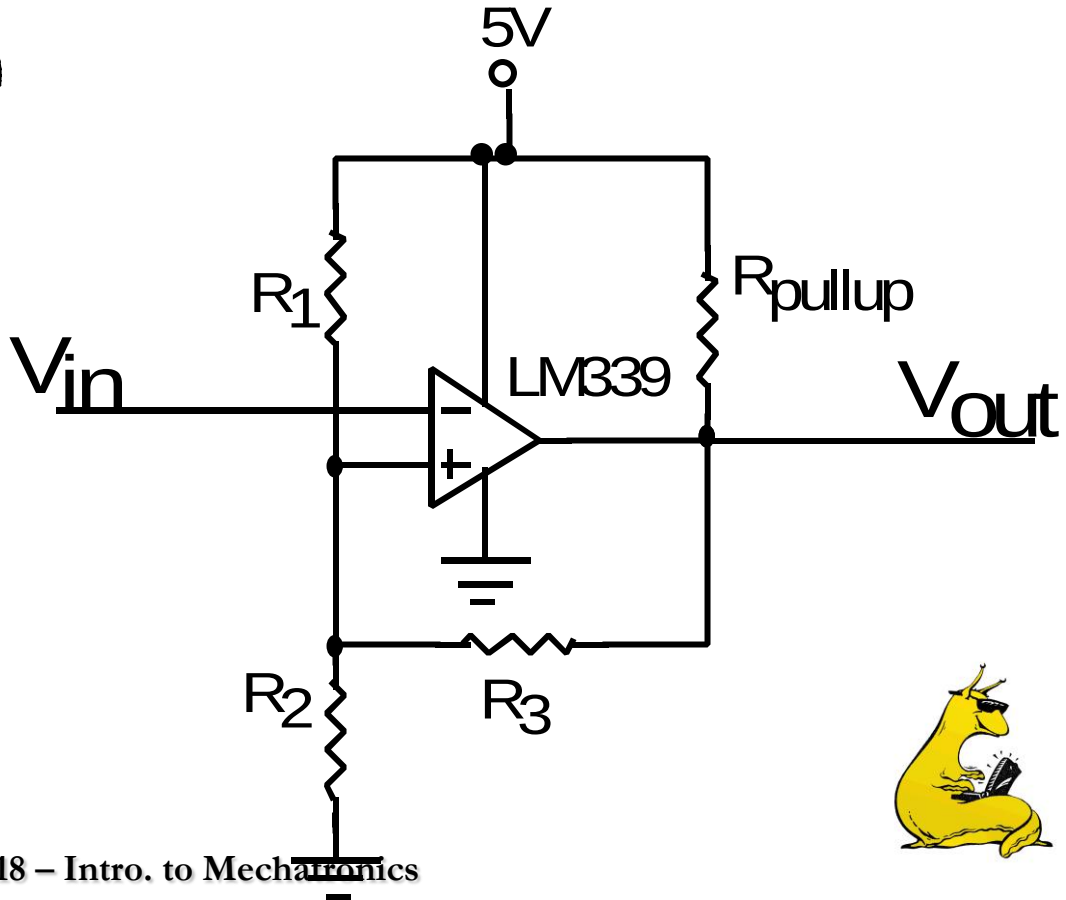
How do you get Hysterisis

1) Schmitt trigger





1) Comparator



National Semiconductor

November 1995

MM54HC14/MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

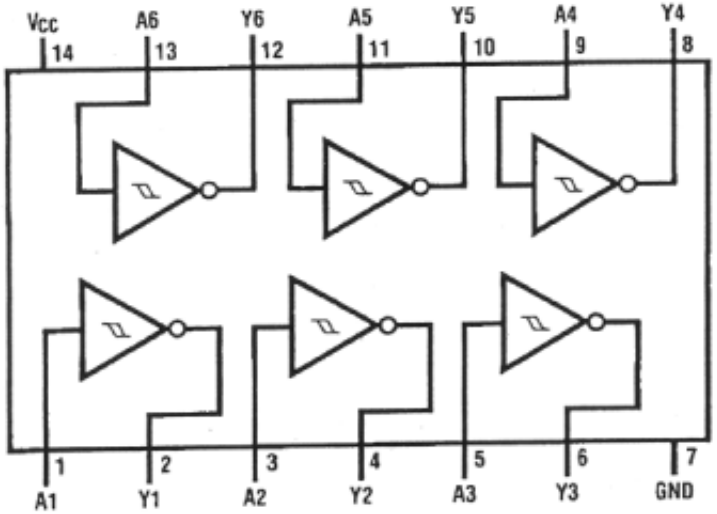
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V

Connection and Schematic Diagrams

Dual-In-Line Package



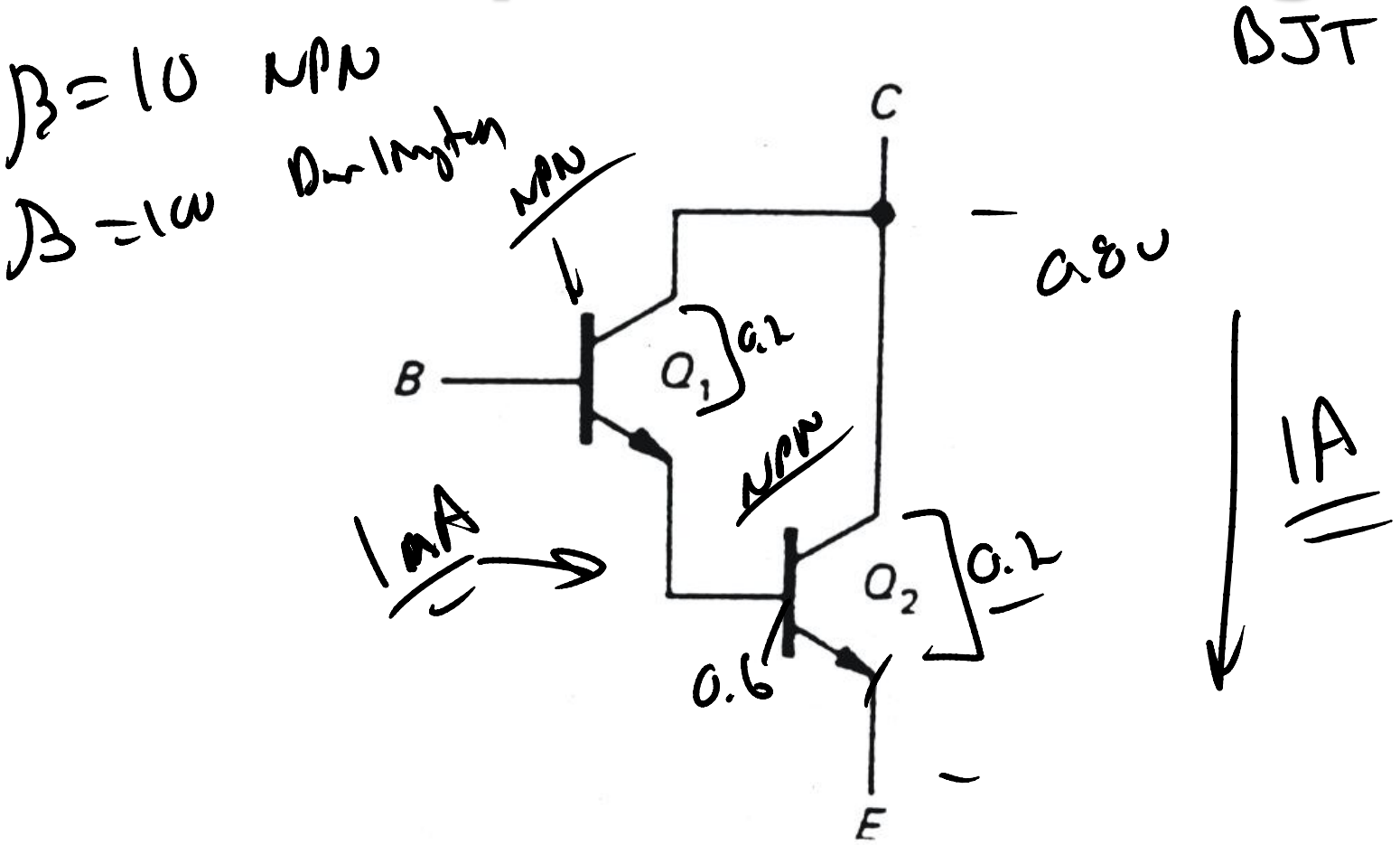
TL/F/5105–1

74HC14

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$		54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	V
			4.5V	2.7	2.0	2.0	2.0	V
			6.0V	3.2	3.0	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	1.0	V
			4.5V	1.8	2.2	2.2	2.2	V
			6.0V	2.2	3.0	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.5	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	1.0	V
			4.5V	0.9	1.4	1.4	1.4	V
			6.0V	1.0	1.5	1.5	1.5	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert = 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IL}$ $\lvert I_{OUT}\rvert = 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert = 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert = 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert = 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert = 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA

Power Outputs: The Darlington



National Semiconductor

March 1995

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

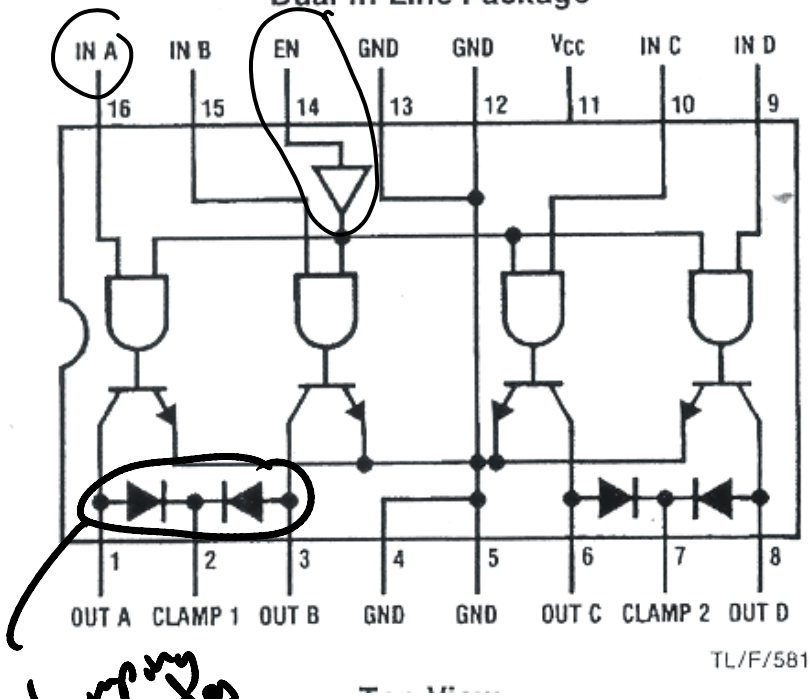
- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

DS3658 Quad High Current Peripheral Driver

DS3658

Connection Diagram

Dual-In-Line Package



TL/F/5819–1

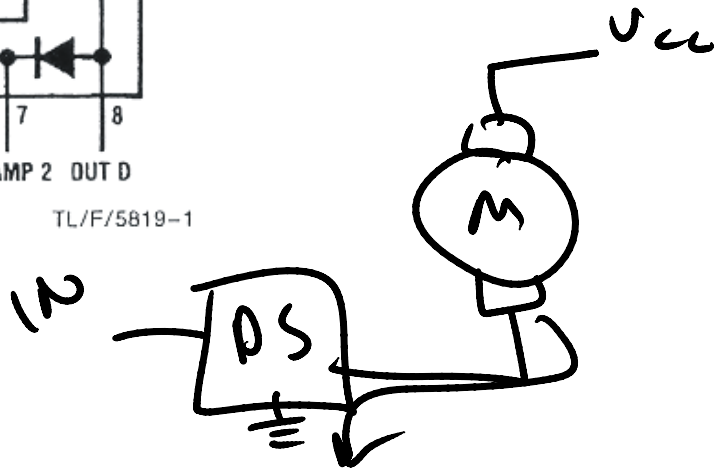
Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state

L = Low state

Z = High impedance state



DS3658

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	10	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.4	V
		I_L = 600 mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	V_{CE} = 70V, V_{IN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.0	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs High		60	85	mA
		All Inputs Low		2	4	mA

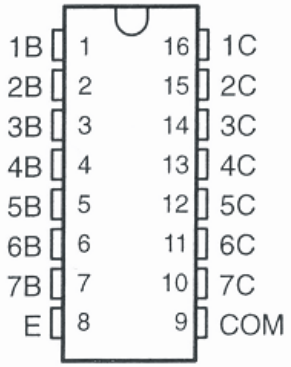
ULN2001A THRU ULN2004A
DARLINGTON TRANSISTOR ARRAYS

SLRS027 – D2624, DECEMBER 1976 – REVISED APRIL 1993

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series

D OR N PACKAGE
(TOP VIEW)

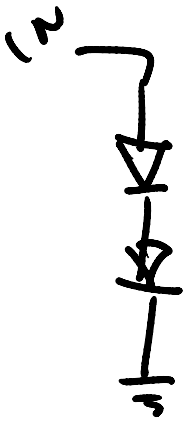


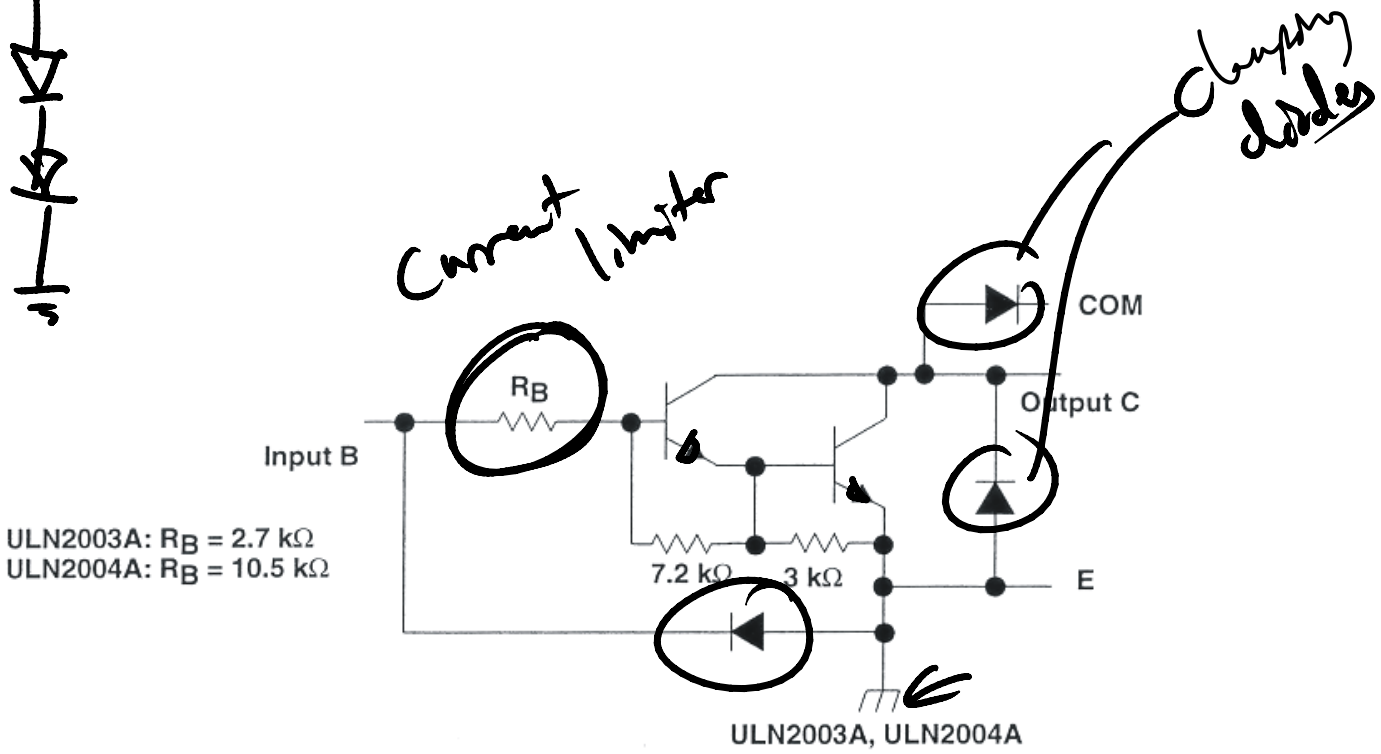
description

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

The ULN2001A is a general-purpose array and can be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

ULN-2003A




Current limiter
clamping diodes
COM
Output C
R_B
Input B
E
7.2 kΩ
3 kΩ
ULN2003A: R_B = 2.7 kΩ
ULN2004A: R_B = 10.5 kΩ
ULN2003A, ULN2004A

ULN2003A Specifications (1.2)

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A MIN	ULN2003A TYP	ULN2003A MAX	ULN2004A MIN	ULN2004A TYP	ULN2004A MAX	UNIT
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		1	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
		2		V_I = 1 V						500	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

TTL

$\beta = 240 - 350$

ULN2003A Specifications (2.2)

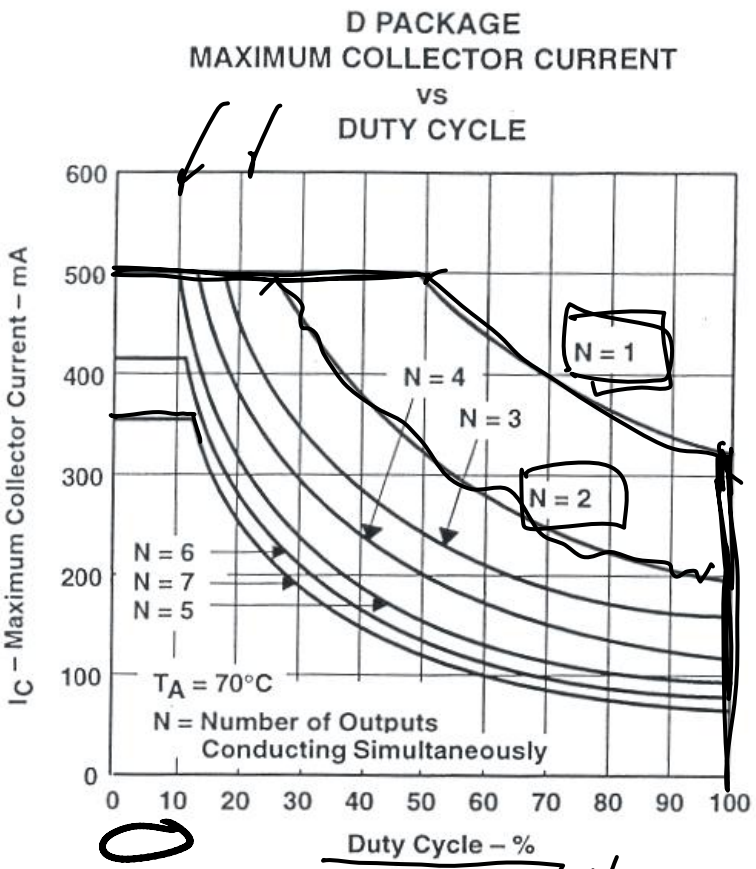


Figure 14

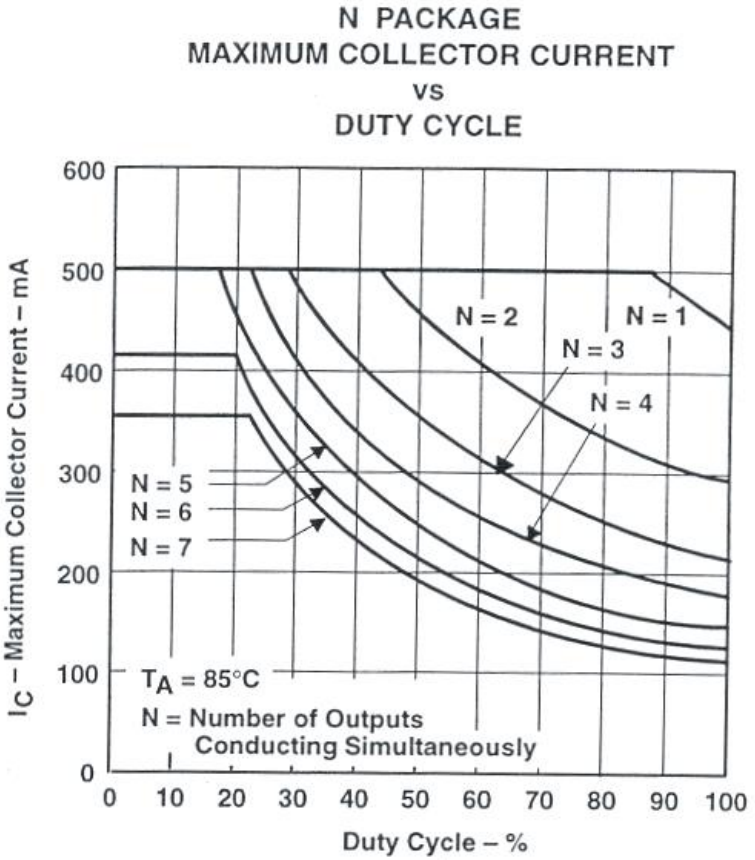


Figure 15

Questions?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