

CMPE 118/L: Introduction to Mechatronics

Cyrus Bazeghi
Winter 2010



Introduction to Mechatronics

- Tu-Th 6:00 – 7:45 PM, JBE 165
- Lab: JBE 115 24/7 access

- Instructor: Prof. Cyrus Bazeghi
- TA: John Burr
- Lab Tutors: Max Dunne, Andrew Hill, Colin Beighley



About Me

- Design engineer and Architect
 - Digital VLSI, System on a Chip, media processors, 3D graphics, memory controllers
- Embedded systems design
 - Microcontroller and FPGA based
 - Animal research, lab equipment, environmental data logging
- Teaching and research
 - CE12, CE13, CE100, CE123A/B, CE222/223
 - Computer Architecture



Class Information

- Please see the class website for the syllabus and “planned” schedule for the quarter.
- www.ucsc.edu/classes/cmpe118/Winter10



Why "Smart Products?"



mechatronics — Japanese

— Focus — MP as component not
as a controller
(No feedback ctrl)

— encompasses

- mechatronics
- embedded systems
 - limited resources
 - cheap!

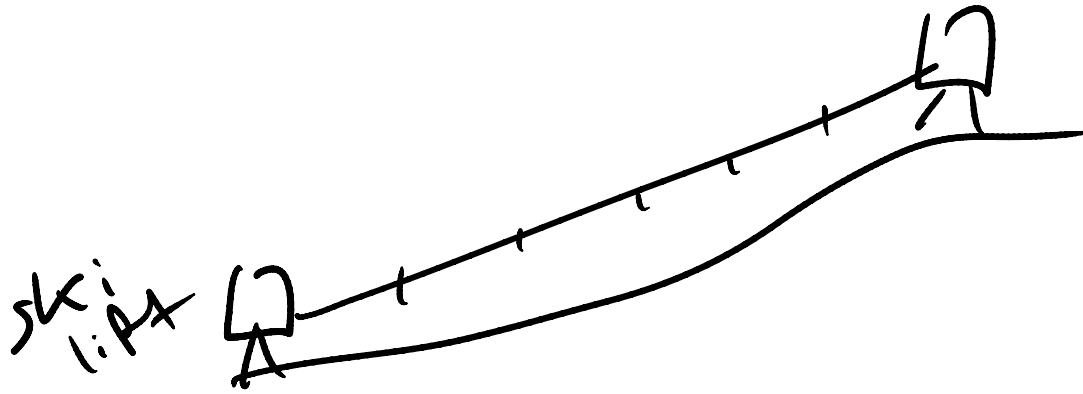


What Makes Mechatronics Different?

- intelligent decision making
- adaptability & reaction

ex: heater in room

- cost eff.



What Makes the Decisions?

Computer - ess. operating of
H's



Where have you encountered Smart Products?

• some are tooth brush

• Automotive ginourms

- mp3

- games

iphone

kitchen App

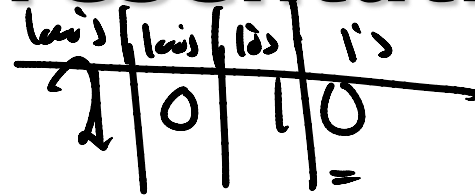
point!

every where

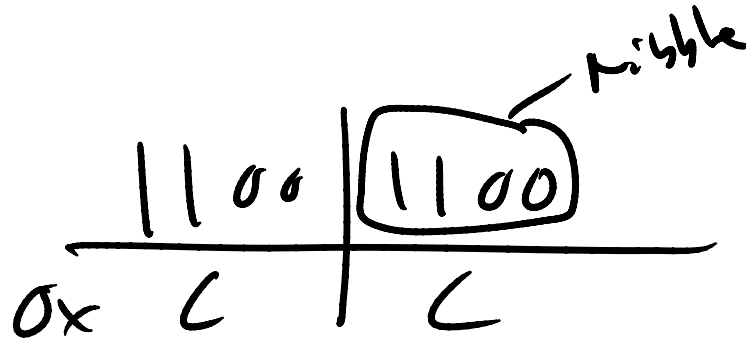
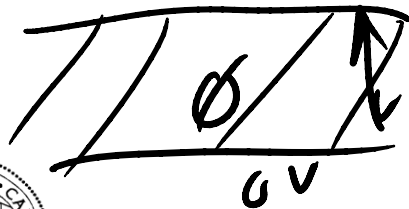
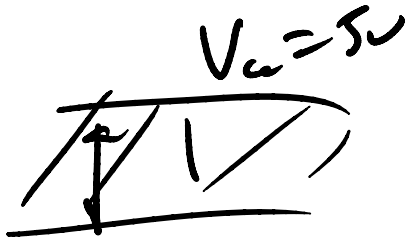
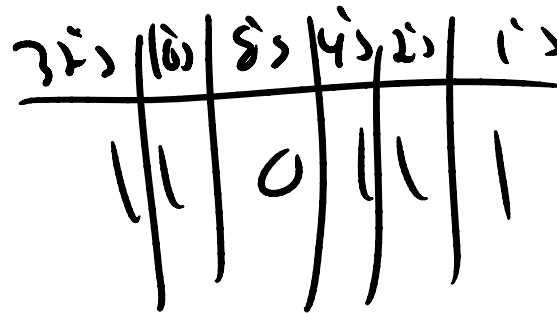


Number Representations

Base 10



Base 2



Number Terminology

bit = unit of info 1 or 0

8bit = byte

T F
on off

byte 8-bit = 2^8 = 256 patterns

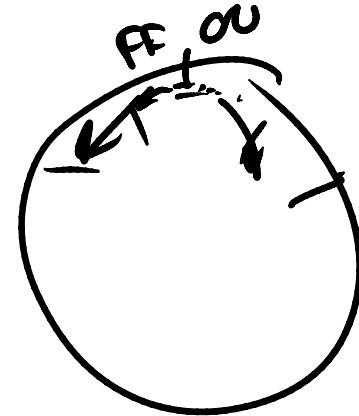
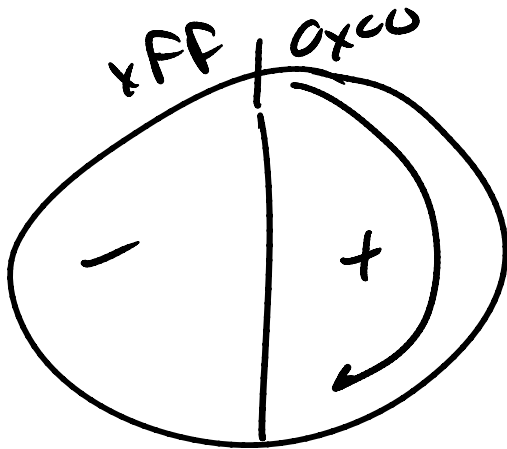
int 16-bit = "word" = 2^{16} 65536 patterns

long 32-bit = 2^{32} = 4 billion

depends on the arch.



Modulo Arithmetic



char a = 100;
 char b = 5;
 char c;

5 x 100
 x 100

$$c = (a * b) / 4$$

$$= 61$$

$$c = ((int)a * b) / 4 \quad \text{type cast}$$



Bit Manipulation (1.2)

Test bit

clear

set

toggle

bit wise op.

AND &

OR |

NOT ~

XOR ^

val = 0110110
 MASK 00000100

00000100

uses MASK's

ex. check if

if define

val & = BIT2Hi

bit [2]

BIT2Hi

BIT2Hi

is set

0x04



Bit Manipulation (2.2)

set bit[2]

val |= BIT2H;

```

val 01100000
     00000100
-----
     01100100
    
```

clear bit[2]

val &= (~BIT2H)

```

val 01100000
     11111011
-----
     01000000
    
```

toggle bit[2]

val ^= BIT2H;

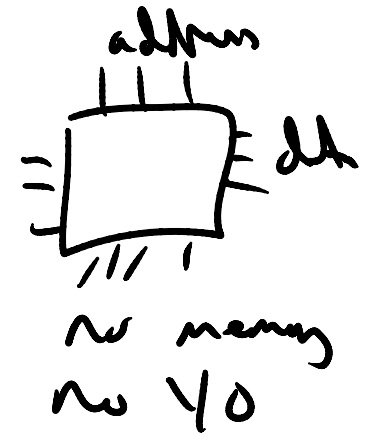
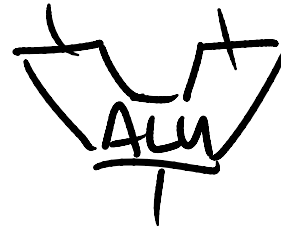
```

val 01100100
     ^ 00000100
-----
     01100000
     ^ 00000100
-----
     01100100
    
```

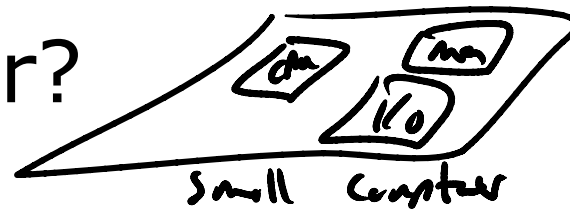


What is a:

- Microprocessor?



- Micro-computer?



- Microcontroller?

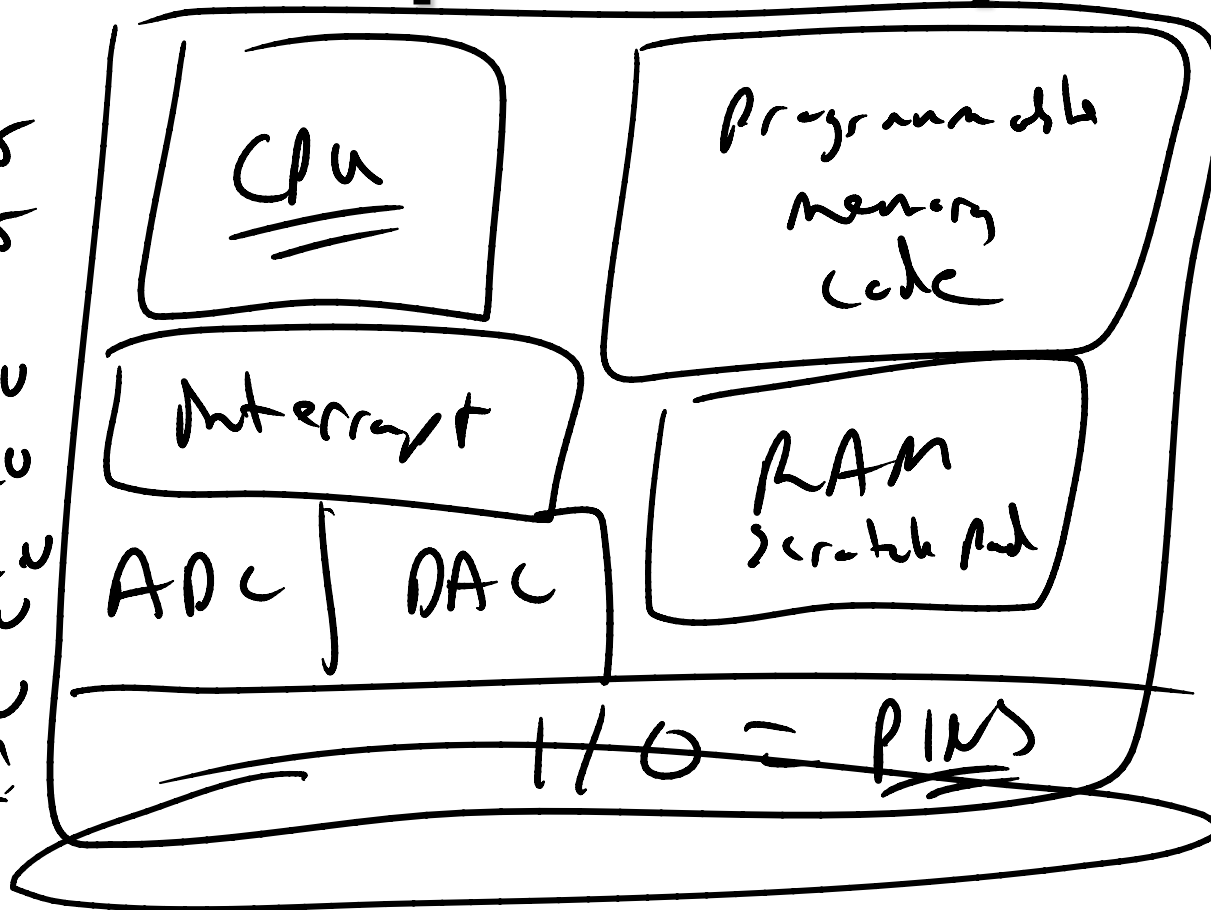
1920's Motorola

CPU, RAM, Flash, ADC, Counter, Timers
single chip



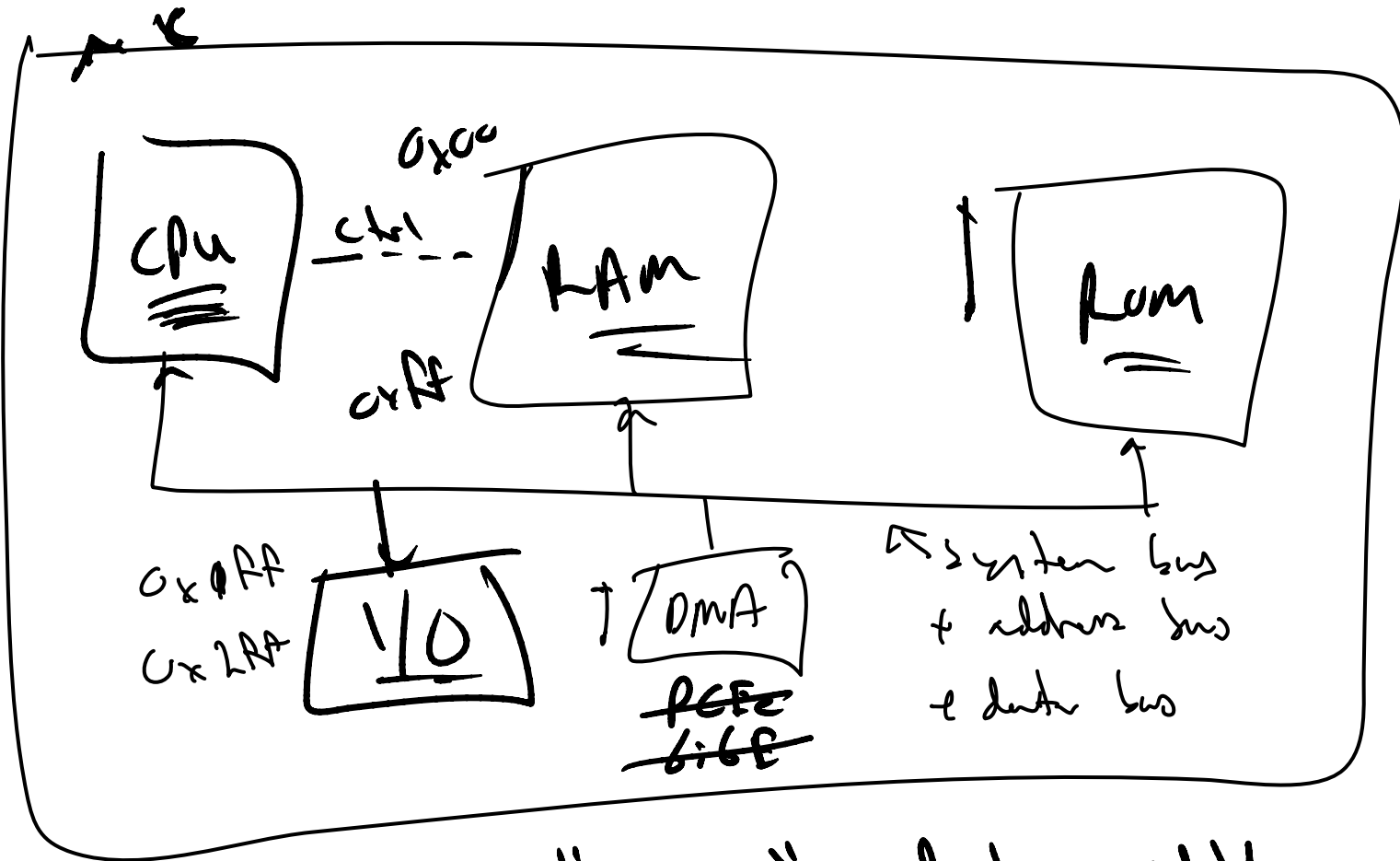
Micro-Computer Components

TTL 0-5
CMOS 0-5
—
0-3.3V
0-2.9V
0-1.9V
0-1.8V
0-0.9V
Power!



Noise margin!



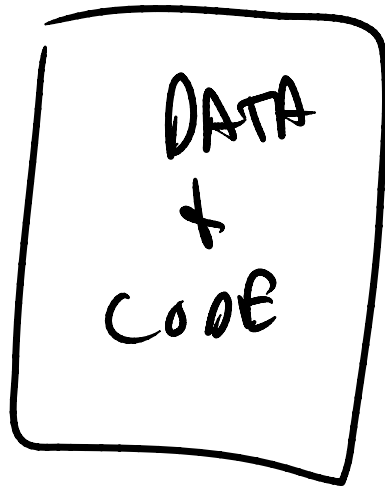


MS430

32-bit
 16-bit
 8-bit
 "bitness" - data width



What's in the Address Space?



instr opcode
DATA
Control reg.
I/O instrs.



Von Neuman
simple & cheap

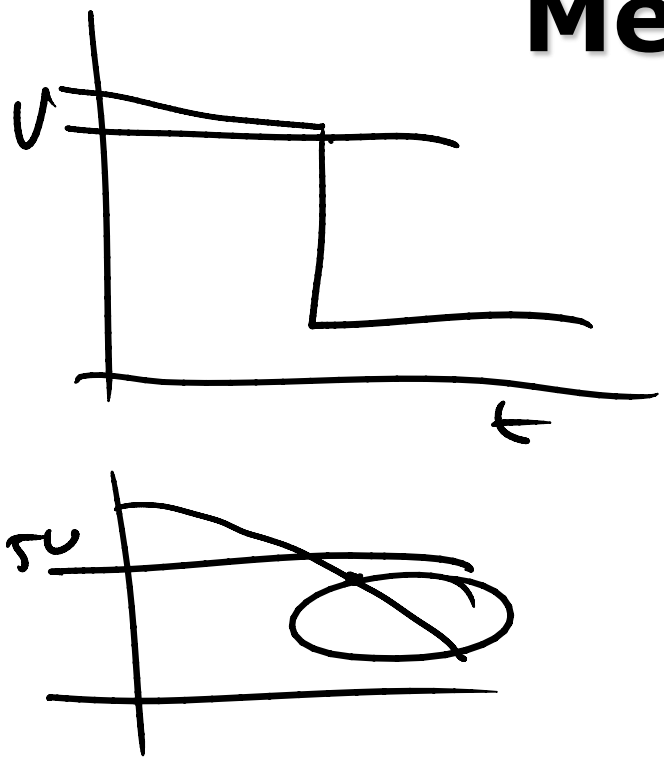
↓
memory mapped I/O.

Harvard
DSP



Memory Map

MC11



Non volatile memory

FFFF		FLASH	EPROM
E000	DFFF		
C000			EPROM
B7FF	B600		E ² PROM
B03F	B000		Registers
8000			
7FFF			
1000			RAM
0100			
00FF			
0000			RAM

32kbs

256 B
16k Vector
table



Program Memory Options

MROM - Masked Read only memory
burned in @ factory.
expensive > 1M

PLM

programmable Read only mem.

EPROM - electronically
programmable...
byte @ a time

erasable



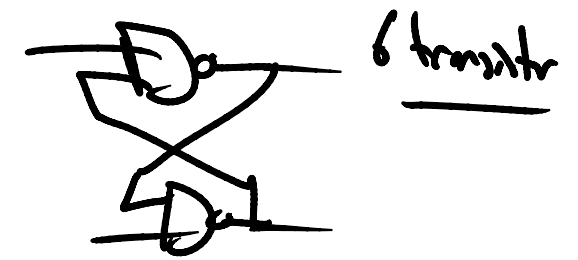
EEPROM - el. erasable ROM
"Flash" - "block" @ a time 512b.



Scratchpad Memory Options

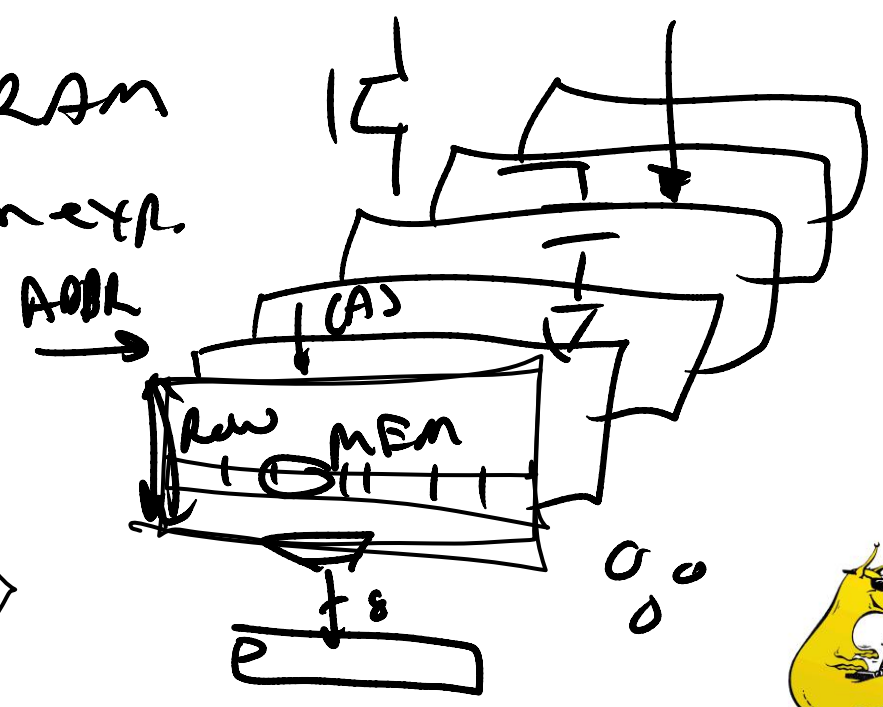
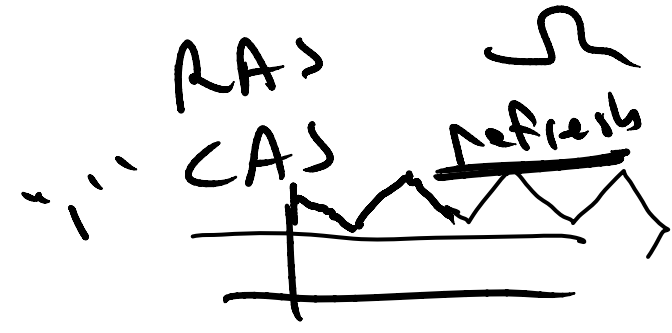
STATIC Mem - SRAM

"very fast" exp.
simple interface.



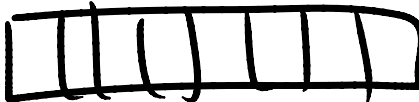
Dynamic mem DRAM

cheap & in exp.
slower



What Features Will You Find? (1.3)

parallel I/O: "ports" memory locations

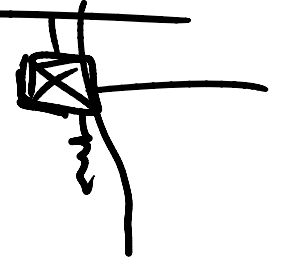
programmable/fixed 

+ dir

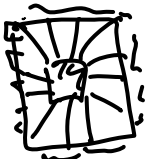
+ pull up

+ pull down

+ tri-state



Pins!!



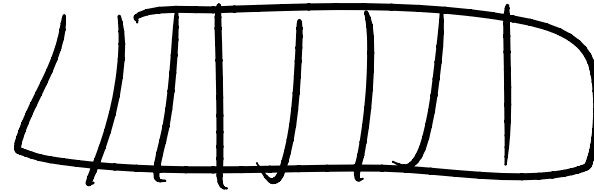
multifunctions

{ ADL or gen I/O }
{ SPI or gen I/O }



What Features Will You Find? (2.3)

Counters



up/down counter

sys. clk as trigger 

events to trigger

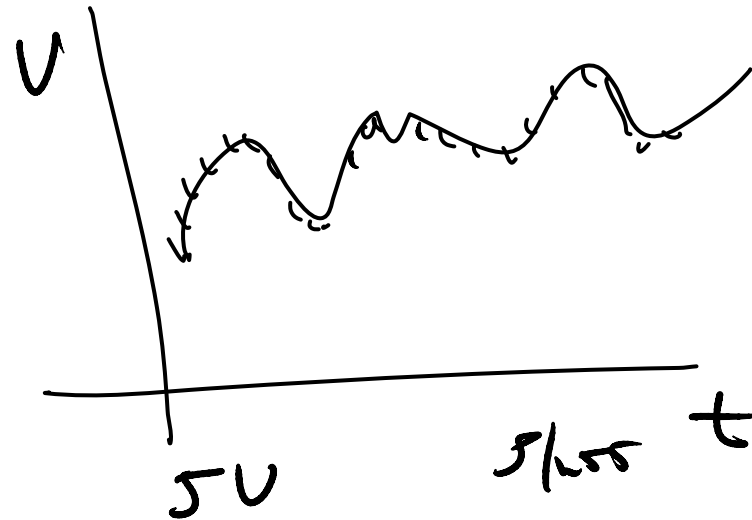
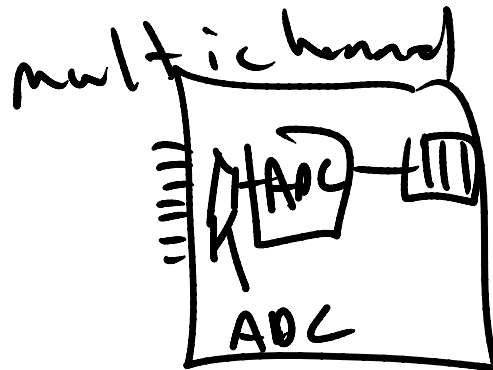
Rabbit
TRC



What Features Will You Find? (3.3)

ADC or A/D

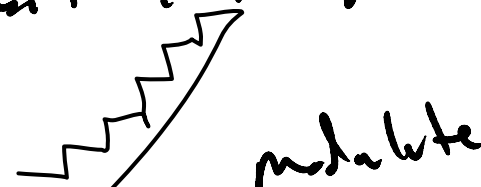
8-bit
10-bit
12-bit



5V
8bit 255 steps \sim 20mV
10bit 1023 steps \sim 5mV

DAC - D/A
pwm

True DAC



modulate



What Features Will You Find? (3.4)

Serial Communication

Synchronous -

SPI

Tx, Rx, Clk, Gnd

Fast

asynchronous
R2L22

- no clock

2 wire tx/rx

band rate

I2C - SDA
SCL



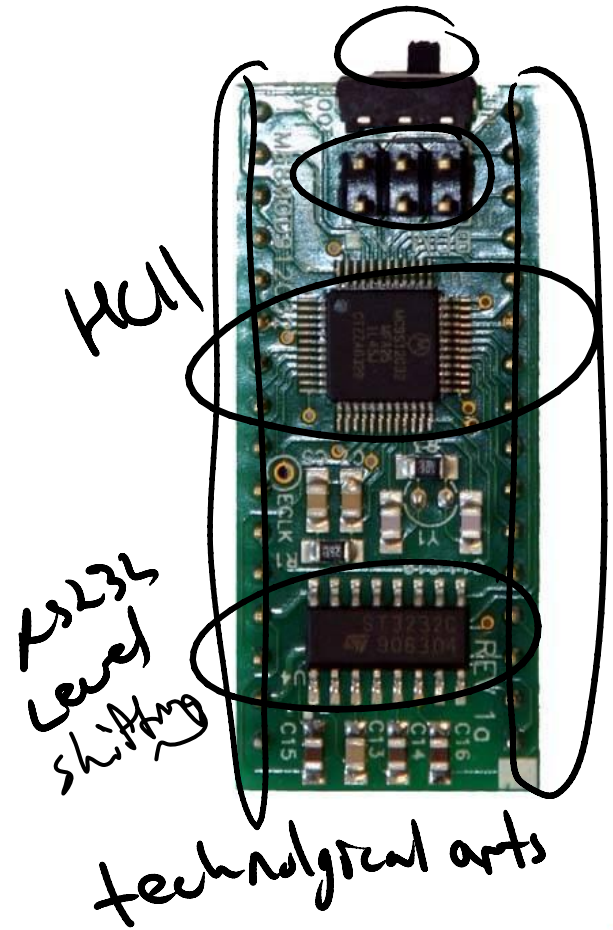
What Differentiates Microcontrollers?

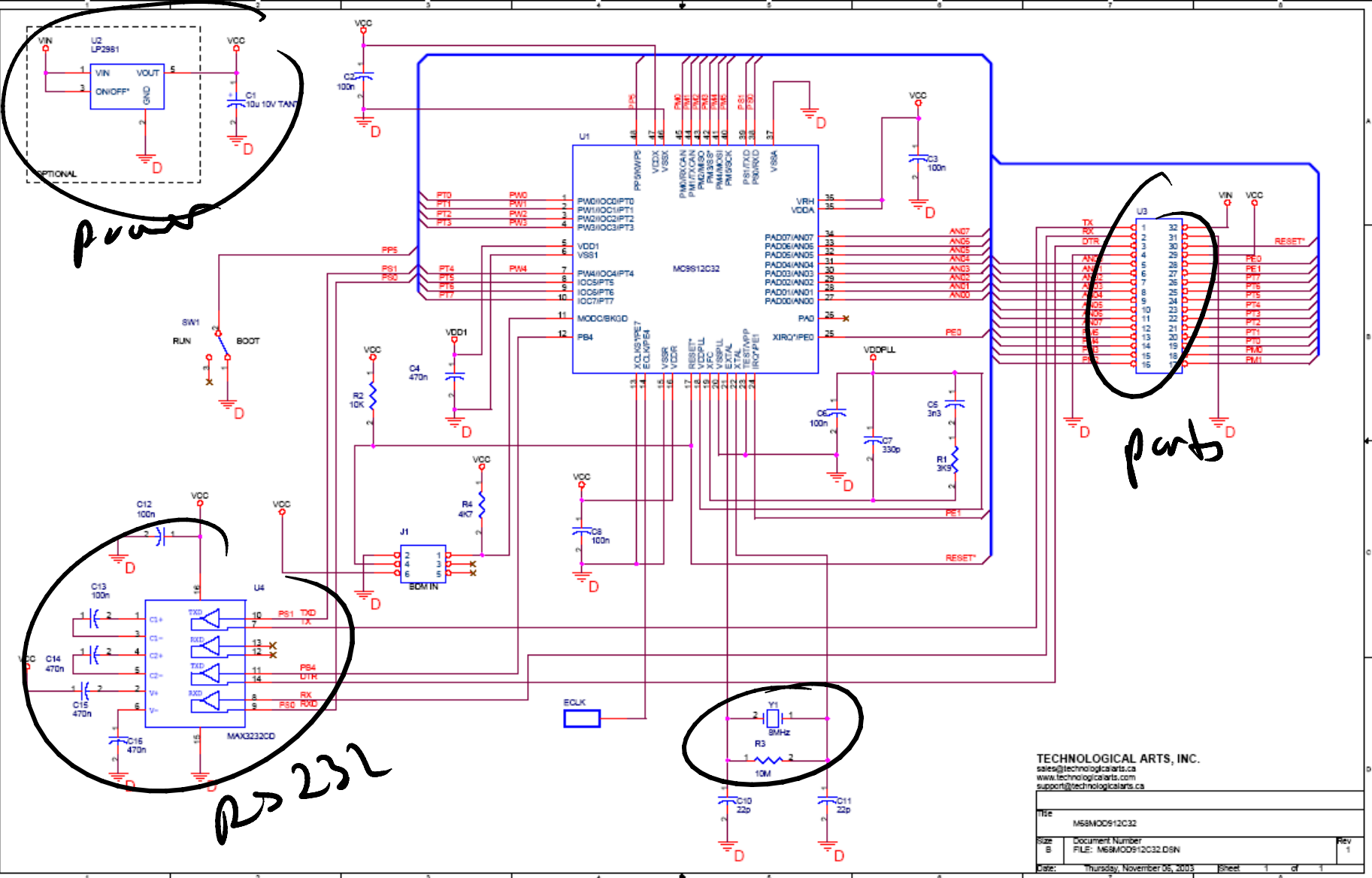
- ① Feature set
 - peripherals
SPI, serial, I²C, CAN, ethernet
 - memory
"bitness"
- ② Architecture
 - 8051
 - 280
 - HLL / (L auto
microcode
"MAC")
 - DSP
- ③ physical size
 - 4 pin D 2mm
 - ~600 pins
 - BGA
- ④ Cost
 - < \$1
 - > \$100



Freescal 68HC12

- ~ 16-bit μP
- ~ C code
- has a stack
- ~ lots of flavors
45





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 www.technologicalarts.com
 support@technologicalarts.ca

File	M68MOD912C32	Rev	1
Size	Document Number		
B	FILE: M68MOD912C32.DSN		
Date:	Thursday, November 05, 2003	Sheet	1 of 1



68HC12 Memory

16 bit address bus 64kB address space
16 bit data bus "bit bus"

2kB RAM - volatile

32kB Flash - code



68HC12 Parallel I/O

24 bi-dir I/O lines

8 multiplexed An by inputs

ADL



68HC12 Timer System

16-bit Free running counter

& input capture \rightarrow \mathbb{F}

& output comparator \rightarrow

set I/O based upon
a count value
Once "configured"
no "code"

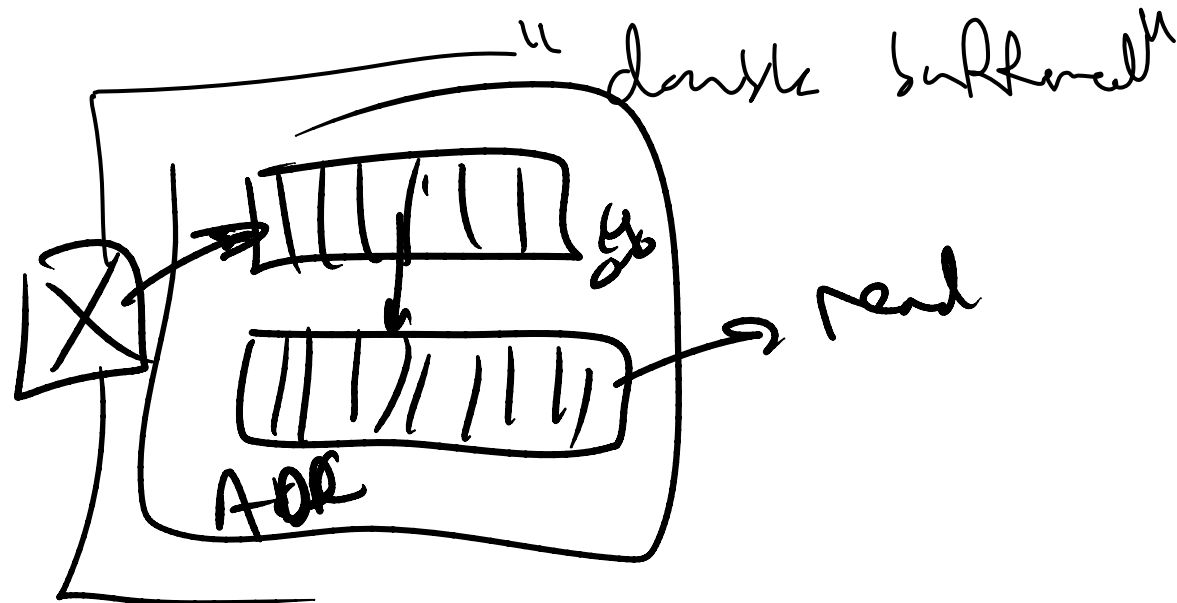


68HC12 A/D Converter

10 bit ADC 5mV @ 5Vref

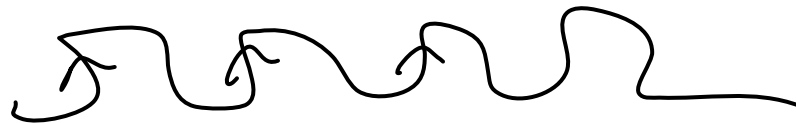
E-channel

2 banks of 4 pins



68HC12 Pulse Accumulator

8/16 bit



Count the full 16 bits



wheels



68HC12 Serial I/O

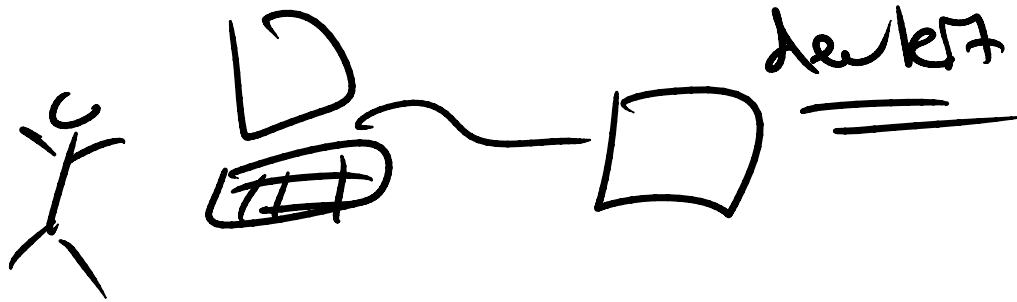
RS232 - TTL levels
level shifting

SPI - 3 wire Master/slave
methods

SCI - Free



The Development Process



Questions?















