University of California, Santa Cruz
Computer Engineering Department
Digital Logic Laboratory

Laboratory 7

I. Description

This laboratory emphasizes engineering design and implementation of a sequential state machine from a written specification.

II. Written Design Problem Specification:

Basic Description

Consider a main road running in a North-South direction and a farm road running East-West that cross forming an "X" intersection where traffic-control signals operate. Both roads have the usual red, yellow and green signals found on poles controlling the four directions. These are controlled by four *forward* sensors, monitoring traffic flow for each of the four directions. The main road also has left-turn control signals, while the farm road does not. Each left-turn traffic control requires one *left-turn* sensor; so, there is one for the North direction (to turn West) and one for the South direction (to turn East). When there are no vehicles on either road, the system will default to North/South flow on the main road. So long as forward-direction traffic subsequently occurs only on the main road, the North/South forward signals will remain green (obviously, the left-turn signals will be red).

Signal Logic

Color changes on any of the six signal poles, four forward and two left-turn, will always operate in the following sequence: Green → Yellow → Red → Green … etc. with time intervals based on realistic California traffic signal behavior: Green → Yellow must be a mininum of one second; Yellow → Red must be three seconds. If all sensors have been tripped at the same time, the order of signals will be: N left-turn, S left-turn, main road forward, farm road.

Farm Road Logic

When a vehicle trips any single farm road sensor, the main road will turn red followed by the farm road signals turning green. Traffic on the farm road will be allowed for up to six seconds without continued tripping of the farm road sensors, or four seconds if a main road sensor has been tripped. With continued tripping on the farm road, the farm road will retain priority for 15 seconds maximum – assuming there is a conflicting sensor trip from the main road. So with continuous farm road traffic, and no conficting main road traffic, the farm road stays green.

Main Road Forward Logic

Logic for the forward sensors will follow the same logic as for the farm road, except that priority will be retained for 20 seconds instead of 15.

Main Road Left-Turn Logic

Each left-turn signal can operate independent of the other, and for each direction, opposing traffic (North or South) must be blocked. When a left turn sensor has been tripped, after the left-turn signal becomes green, it will stay that way for three seconds before changing while no additional left turn traffic is detected. With continued tripping of the left-turn, it will retain priority for 15 seconds maximum – assuming there is a conflicting sensor trip.

III. Implementation:

Design a synchronous finite state machine hardware solution that satifies the overall written specification using the Altera CPLD. The output should employ the two 7-segment displays and the plain red leds available to the CPLD. You can also obtain colored LED's from Bels if you want. Sensor inputs should be assigned to the dip switches. Also, employ one of the dip-switches be used for a reset that turns the two main forward lights green and everything else red.

Spend some time really understanding what's going on with the traffic flow. Use state diagrams first before creating a state table. You may use a combination of VHDL and schematic capture, and consider how decomposition might help you. Note that your engineering notes must reflect all work done to solve/design this problem.

Rather than starting out using CLOCK_DIV to obtain clock signals, consider debouncing one of the Altera board's push-buttons to use as a clock during debugging and verification. After things are working you can then replace it with a periodic clock signal.

Note: you may work with a partner if you wish (however, no more than 2 people per group). Each of you will still be required to submit separate reports written in your own words, but schematics, simultions etc. may be copied and used commonly between you . Moreover each student must separately demonstrate the project and be capable of defending all aspects of its design. Carefully note any additions or changes specifically given by your TA regarding implementation details. Besides the general discussion, your report must contain the final circuit design and any other specific information, like simulations, that your TA might require. Engineering notes should fully support your work and also contain an entry made by your TA indicating a fully (or partially) working circuit design.