STOC(Milwaukee 1981), 312-317.

OPTIMAL WIRING BETWEEN RECTANGLES

Danny Dolev†
Kevin Karplus‡
Alan Siegel
Alex Strong‡
Jeffrey D. Ullman††
Stanford University

ABSTRACT

We consider the problem of wiring together two parallel rows of points under a variety of conditions. The options include whether we allow the rows to slide relative to one another, whether we use only rectilinear wires or arbitrary wires, and whether we can use wires in one layer or several layers. In almost all of these combinations of conditions, we can provide a polynomial-time algorithm to minimize the distance between the parallel rows of points. We also compare two fundamentally different wiring approaches, where one and two layers are used. We show that although the theoretical model implies that there can be great gains for the two-layer strategy, even in cases where no crossovers are required, when we consider typical design rules for laying out VLSI circuits there is no substantial advantage to the two-layer approach over the one-layer approach.

I. Definitions

One useful structure to place on VLSI circuits is a hierarchy of rectangles, where two or more are wired together to form a larger rectangle, which is the smallest rectangle that circumscribes them. [J] is an example of such an approach. In order to make the circumscribing rectangle as small as possible, we must wire together *ports*, which are points on the borders of the rectangles, in some designated order, which we shall generally assume is the same for both rectangles; that is, no crossovers are mandated. We shall assume, as seems sensible, that the ports of two rectangles that need to be wired together are placed on the adjacent sides of those rectangles, as suggested by Fig. 1.

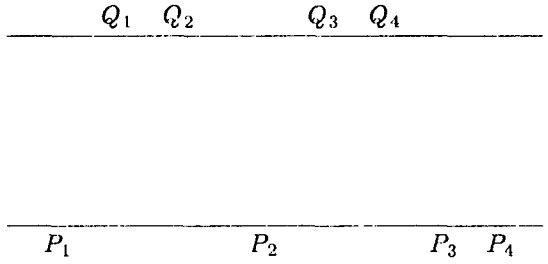

Fig. 1. Basic wiring problem.

The wiring problem, in the abstract, is to draw lines between each P_i and its corresponding Q_i, subject to the constraint that no two lines ever come within one unit of each other. It is therefore sensible to assume that the P_i's are spaced at least one unit from one another, and likewise the Q_i's. Partly for mathematical convenience, and partly to model the fact that within the rectangles there may be unknown wires that we must not approach too closely, it is also assumed that within one unit of the upper and lower lines in Fig. 1, we may only have wires that travel vertically to a port. We consider principally two models for the behavior of wires.

1. Wires can travel in any direction. This case was considered by [T], and an optimal wiring was obtained for the situation where the relative position of the rectangles is fixed both horizontally and vertically, or fixed only horizontally. We call this case of wire behavior the *general case*.
2. Wires can travel only horizontally or vertically. This case, which has been considered by [V, FP, St], for example, is motivated by the fact that many mask-making facilities permit only designs that are composed of horizontally or vertically oriented rectangles. To avoid some complexity in the description of results, we shall assume in this case that the plane is a unit grid, as in [V], and that

† Work supported by a Chaim Weizmann postdoctoral fellowship and DARPA contract MDA903-80-C-0102.
‡ Supported by a fellowship from the Hertz Foundation.
†† Work partially supported by DARPA contract MDA903-80-C-0102 and NSF grant MCS-79-04528.

Permission to copy without fee all or part of this material is granted provided that the copies are not made or distributed for direct commercial advantage, the ACM copyright notice and the title of the publication and its date appear, and notice is given that copying is by permission of the Association for Computing Machinery. To copy otherwise, or to republish, requires a fee and/or specific permission.
©1981 ACM 0-89791-041-9 /80/0500/0312 $00.75

wires can travel only along grid lines. Also, the ports are placed only on grid lines, although not necessarily on consecutive lines. We call this case the *rectilinear case*.

Much of what we say goes through for a larger class of constraints on how wires may travel. For example, we can generalize the rectilinear case to the situation where wires may also travel along the diagonals of the squares of the grid. This model also reflects the real constraints of some mask-making facilities.

Next, let us introduce the kinds of optimization problems we consider. We call the horizontal displacement of Q_1 from P_1 in Fig. 1 the *offset*, and we refer to the distance between the two rows of ports as the *separation*.

1. Given an offset and a wiring rule (e.g., rectilinear), what is the minimum separation for which a legal wiring exists? This is the *separation problem*.
2. Given a wiring rule, for what offset is the separation minimized? This is the *offset problem*.

The last dimension along which we divide wiring problems is the number of layers in which wires are allowed to run. We consider single-layer wirings first. Even though we shall discover that in the rectilinear model, single-layer wirings can be arbitrarily bad, we also show that when the grid is translated into real circuit parameters the single-layer wiring technique appears as good as any other.

We shall also consider two-layer wirings, because these are more general, and are necessary in the situation where the ports of the two rectangles are not to be connected in order (a situation we shall mention only briefly). The optimal wiring problem for this case is claimed in [L] to be $\mathcal{NP}$-complete, but a slight change in the wiring model eliminates that difficulty. In particular, we shall, in the rectilinear case, assume that one layer is reserved for horizontal wires and the other for vertical wires. Further, we assume that two wires can run along a grid line in the vertical direction, but only one in the horizontal direction.† We call this model the *restricted two-layer model*.

II. The Rectilinear Model Separation Problem

Given a fixed offset, and n pairs of ports,

$$(P_1, Q_1), \ldots, (P_n, Q_n)$$

where we take P_i to be both the name of a port on the bottom row and the horizontal position of that port, and we take Q_i to be a similar port on the upper row, we may attempt to find the minimum separation for which a legal wiring exists. Let us define a *right block* to be a maximal sequence of pairs of ports $(P_i, Q_i), \ldots, (P_j, Q_j)$ such that for $i \leq k \leq j$,

1. $Q_k \geq P_k$, and
2. $P_k \leq Q_{k-1}$ if $k > i$.

Condition (1) says that all the connections in the block have the position in the upper row to the right of the corresponding position on the lower row, and condition (2) says that there is some "interaction," that is, each wire competes for horizontal position with its neighbors in the block.

We may define a *left block* in the obvious, symmetric way. We call a left or right block a *block*.

There are two important constraints that force large separations. First, there is the *crossing number* at any horizontal position h. That is the number of values of i for which $P_i \leq h$ and $Q_i \geq h$ or $P_i \geq h$ and $Q_i \leq h$, but not $P_i = Q_i = h$. Second is the *conflict number* for any two pairs of ports, i and j, which we denote by $W(i,j)$ and define as follows. First, $W(i,j) = 0$ in any of the following three cases.

1. $i = j$ and $Q_i = P_j$.
2. $i < j$ and $Q_i - i \leq P_j - j$.
3. $i > j$ and $Q_i - i \geq P_j - j$.

In all other cases, $W(i,j) = \mid i - j \mid + 1$.

Intuitively, the crossing number tells how many wires must cross the vertical line at position h. The conflict number for i and j is intended to measure the number of wires that must cross an imaginary line from P_j to Q_i. This concept is an adaptation of the basic idea of [T] to the rectilinear case. The reason it takes the strange form it does is that the wires may pass either horizontally or vertically between P_j and Q_i. If Q_i and P_j are sufficiently far apart, horizontally, then the wires could pass vertically, and we cannot assert anything about the minimum separation. Thus $W(i,j) = 0$. If Q_i and P_j are close, horizontally, then the wires cannot all pass vertically, and we can show that one channel per wire in the horizontal direction will be needed. In this case, a lower bound on the separation can be obtained.

Example 1: Figure 2 shows an interesting case, where n pairs of ports are offset one unit. At any interior horizontal position the crossing number is 2. However, $P_n - Q_1 = n - 2$, which is less than $n - 1$. Thus, $W(1,n) = n$, from which we shall conclude that separation n is required. []

Lemma 1: The largest crossing number in a problem is never greater than the largest conflict number. []

Lemma 2: In any one-layer solution to a rectilinear separation problem except the *trivial* problem ($P_i = Q_i$ for all i), the number of *channels* (grid lines between the lines of ports) is at least as great as the largest conflict number.

† In terms of nMOS [MC] circuits, we are modeling an arrangement where metal wires run horizontally and polysilicon and diffusion wires run vertically. As crossovers between wires of the latter types forms a transistor, it is fortunate that in the designs we use, such crossovers do not occur. In principle, we could negate the effect of the transistor by "implanting" the region of crossover, but the result is an undesirably high resistance.

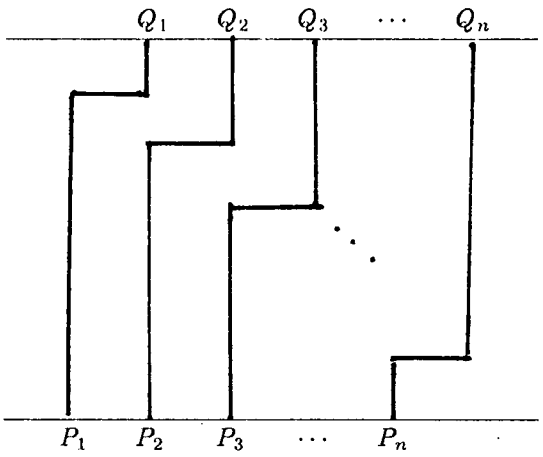

Fig. 2. Example showing large conflict number and small crossing number.

Proof: Adapts the ideas of [T]. []

Theorem 1: In any rectilinear separation problem, a number of channels equal to the largest conflict number is necessary and sufficient for a one-layer wiring to exist.

Proof: With Lemma 2, we have only to give an algorithm that achieves the bound. First, break the pairs of ports into blocks, that is, maximal sequences of left-going and right-going pairs. To wire any block we use a greedy algorithm. Say the block is a right block. Then starting at the left end, we run wires across from bottom to top. When, as we lay any particular wire, we cannot proceed vertically, we move to the right instead, returning to the vertical direction when legally able to do so. []

Example 2: Figure 2 is an example of an application of the greedy algorithm. []

Corollary 1: There is always an optimal solution to the rectilinear separation problem in which the wires for a block do not overlap in the horizontal direction with the wires for any other block.

Proof: The greedy algorithm provides such a solution. []

Corollary 2: The number of channels needed for the rectilinear separation problem can be determined in $O(n)$ time.

Proof: Normalize the problem so all blocks are right blocks by redefining

$$P_j = min(P_j, Q_j)$$

and

$$Q_j = max(P_j, Q_j)$$

By Corollary 1 this doesn't change the number of channels needed. Let c_j be the smallest $i \leq j$ such that $P_j - Q_i \leq j - i$ (or j if no such i). By definition of W, $W(c_j, j) = max_{1 \leq i \leq j} W(i, j)$. Since both $P_j - j$ and $Q_i - i$ are nondecreasing functions of j and i, respectively, $c_j \leq c_{j+1}$. Thus we can find the maximum conflict number by incrementing j from 1 to n, searching for c_j (starting at c_{j-1}) and computing $W(c_j, j)$. []

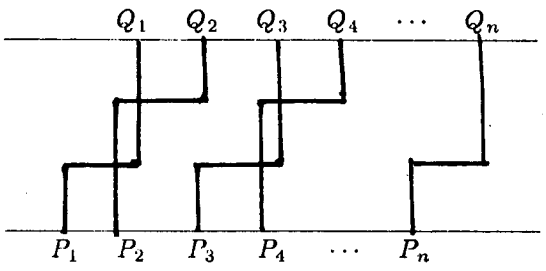

Fig. 3. Two-layer greedy wiring

When we consider the restricted two-layer model, we get an entirely different sort of result. There, the conflict number is irrelevant, and only the crossing number influences the separation.

Lemma 3: A number of channels equal to the largest crossing number is necessary for a restricted two-layer solution to the rectilinear separation problem to exist. []

Theorem 2: A restricted two-layer solution to the rectilinear separation problem using no more channels than the largest crossing number exists.

Proof: We use the following strategy. First, as in Theorem 1, break the pairs of ports into blocks. All wires in a block run first vertically in one layer, then horizontally in the second, and finally vertically again in the first layer. Say we are wiring a right block. Then we select channels from left-to-right. In each case, pick the lowest available channel for the horizontal wire.

If $P_j = Q_i$, and the j^{th} pair uses a higher channel than the i^{th}, then we have two vertical wires in the same place. This problem is avoided, by making the grid spacing large enough to handle two wires†. []

Example 3: In Fig. 3 we see a wiring of the problem of Fig. 2, using the greedy algorithm of Theorem 2. []

III. The Rectilinear Offset Problem

We now consider how to select the offset that minimizes the separation. Given any offset, we know how to produce an optimal one-layer wiring in $O(n^2)$ time and an optimal two-layer wiring in $O(n)$ time. In fact, we can calculate the separation (without the wiring) in $O(n)$ time in either case. However, in order to obtain a polynomial-time algorithm for the offset problems, we must limit the number of offsets that must be tried. The following fact is useful.

Lemma 4: The maximum crossing number and the

† In practice we can use a third color to obtain a somewhat smaller grid spacing, yet not create any transistors.

maximum conflict number are convex functions of the offset. []

The following observations are also useful.

Lemma 5: Sliding the upper row of a right block to the right cannot decrease the crossing or conflict numbers, and analogously for sliding left blocks left. []

Lemma 6: As we slide the upper row of ports left or right, the crossing numbers only change at positions where $P_j = Q_i$ for some i and j, and conflict numbers only change at offsets where $P_j - j = Q_i - i$. []

Theorem 3: There is an $O(n \log n)$ algorithm to solve the rectilinear one-layer and restricted two-layer offset problems.

Proof: (sketch) We shall only prove the one-layer case. The restricted two-layer case is similar. To begin, suppose we pick some particular offset and calculate the minimum separation. Call a block *critical* if it has a conflict number as large as any in the whole problem. Observe that if the offset chosen yields a critical left block and a critical right block, then by Lemma 5, we are done. Suppose all critical blocks are right blocks. Then we can only improve the separation if we slide the upper row left. Similarly, if we try some offset and find only critical left blocks, we need only consider sliding the upper row right.

If the P's and Q's are bounded by a polynomial in n, then the optimal offset must be polynomial in n, and a binary search provides the optimal offset in $0(\log n)$ stages, where we calculate the separation once at each stage. Since the latter calculation takes $0(n)$ time, we have an $0(n \log n)$ algorithm.

However, we can compute the optimal offset in $0(n \log n)$ time even when the positions of the ports are arbitrary, by doing a binary search involving the n^2 critical offsets indicated by Lemma 6. To begin, assume that $Q_1 = P_1 = 1$ and that zero offset occurs when Q_1 and P_1 are aligned. Define $D(i,j) = P_j - Q_i - j + i$; that is, $D(i,j)$ is the displacement when Q_i is moved to position $P_j + i - j$, which is one of the critical offsets indicated by Lemma 6.

We compute d_{low} and d_{high}, the lowest and highest offsets between which we know the optimal offset to lie. Initially, $d_{low} = -Q_n + n$ and $d_{high} = P_n - n$. Repeatedly find d between d_{low} and d_{high} such that at least one-fourth of the i-j pairs for which $D(i,j)$ lies between d_{low} and d_{high} lie on either side of d. We shall require only $0(n)$ time to compute d, as well as $0(n)$ time to compute the separation at d and tell on which side of d the optimum point lies. As we start with n^2 possible offsets and have at most three-fourths as many possibilities after each stage, $0(\log n)$ stages suffice, and we have an $0(n \log n)$ algorithm.

To find the desired d, we shall compute LOW(j) and HIGH(j), where

$$\text{LOW}(j) = \min\{\, i \mid D(i,j) \geq d_{low} \,\}$$

or $n+1$ if no such i exists, and

$$\text{HIGH}(j) = \max\{\, i \mid D(i,j) \leq d_{high} \,\}$$

or 0 if no such i exists. We compute LOW in $0(n)$ time by

```
i:=1;
for j:=1 to n do begin
    while (i ≤ n) and (D(i,j) < d_low) do
        i:=i + 1;
    LOW(j):=i;
end
```

The reason the above works correctly is that $D(i,j)$ is monotonically nondecreasing in i and nonincreasing in j. Of course, HIGH can be computed similarly in linear time.

Define, for $1 \leq j \leq n$

$$m_j = (\text{HIGH}(j) + \text{LOW}(j))/2$$

and

$$d_j = D(m_j, j)$$

and let d be the weighted median of the d_j's, where the weight of d_j is the number of possible offsets involving P_j, that is, 1+HIGH(j)—LOW(j), except in the case where LOW(j)=$n+1$ and HIGH(j)=0, i.e., there is no $D(i,j)$ in the range d_{low} through d_{high}. In the latter case, the weight is appropriately zero. We can compute the weighted median in linear time by a generalization of the usual algorithm apparently due first to Bentley and Shamos; see [Sh]. Then approximately three-fourths, at most, of all the $D(i,j)$'s that are in the range d_{low} through d_{high} are in the interval d_{low} through d or the interval d through d_{high}. []

The following fact is not surprising, but worth mentioning.

Theorem 4: The separation problems are log-linear reducible to their corresponding offset problems.

Proof: Given a separation problem, pick a position to the left of all the points, and mirror the problem about the vertical line at that point. By Lemma 4, and a simple symmetry argument, the new data (the original points plus their mirror images), treated as an offset problem, has an optimal solution with no change in the offset. []

IV. Comparison of One-Layer and Two-Layer Solutions

Looking at Figs. 2 and 3, one gets the impression that two-layer wirings can be arbitrarily better than one-layer wirings. However, we shall argue that such is

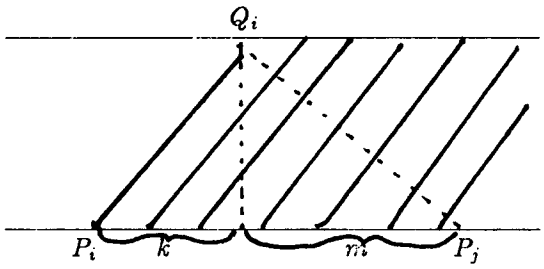

Fig. 4. Diagram for Theorem 5.

not the case in practice. We need a preliminary result saying that as long as ports are not packed too tightly along the lines, then a one-layer solution with separation proportional to the crossing number, not the conflict number, always exists.

Theorem 5: Let x be the maximum crossing number. Suppose there is a constant $\alpha > 0$ such that for every $r \geq x(1 + 1/\alpha)$, no r consecutive grid lines have more than $r/(1 + \alpha)$ ports. Then there always exists a one-layer solution to the rectilinear separation problem using no more than $x(1 + 1/\alpha)$ channels.

Proof: (sketch) The crucial case is the one shown in Fig. 4. Note that k is the crossing number at Q_i (thus $k \leq x$) and $k + m$ is the conflict number $W(i, j)$ if the latter is not zero. We must show that $W(i, j)$ is either proportional to x or is zero, thus showing that the maximum conflict and crossing numbers are proportional. If $m \leq x/\alpha$, then $W(i, j)$ is no larger than $x(1 + 1/\alpha)$. If $m > x/\alpha$, reason as follows. In order that $W(i, j)$ not be zero, we must have $k + m \geq P_j - Q_i$. But by our assumption about the sparseness of ports, we can show that $m \leq (P_j - Q_i)/(1 + \alpha)$. It follows from these two inequalities that $k + m \geq m(1 + \alpha)$, or $m \leq k/\alpha$. Since we assumed $m > x/\alpha \geq k/\alpha$, we see that $W(i, j)$ must be 0. []

Note that there is a qualitative difference between the situation where ports are not as densely packed as the grid lines, however close to one the ratio may be, and the case where ports are packed one to a grid line. In the former case, the separation depends on the crossing number only, and in the latter on the conflict number.

Now we can apply Theorem 5 to particular values of α that reflect real design rules. First, in terms of λ, the fundamental unit for design rules, We can run a single-layer wiring in red (polysilicon) with grid units equal to 4λ†. However, consider the grid size for a two-layer wiring. Assuming that wires run vertically in red, horizontally in blue, then vertically in red†, according to the algorithm of Theorem 2, we have several choices, none very good.

Example 4: We could use a horizontal grid of 10λ and a vertical grid of 7λ. That is, we require that ports be separated by 10λ. But if that is the case, we could use a 4λ grid and a one-layer wiring, and claim that $\alpha = 3/2$. Then, by Theorem 5, there is a wiring with no more channels than 5/3 the maximum crossing number. If x is that maximum, then in terms of λ, the separation in the one-layer case is $6.67\lambda x$, while for the two-layer case, with its 7λ vertical grid, we need $7\lambda x$ separation, which is greater. []

We could also use a three-color wiring with an 8λ horizontal grid and 7λ vertical, which gives slightly better separation than the one-layer solution. Other choices for the grid size in the two-layer case, such as a 7λ horizontal grid coupled with a 14λ vertical grid, yield the same conclusion: in practice. one-layer wirings are as good or better than restricted two-layer wirings. Note that we cannot prove the 8 by 7 or 7 by 14 grids to be best possible for their horizontal grid values, so we must leave open the possibility that better grids could be discovered and our conclusion about restricted two-layer wirings contradicted.

V. Other results

We shall summarize some of the other results related to wiring problems of the nature we have discussed.

Theorem 6: We can solve the rectilinear one-layer and two-layer offset problems in $O(n^3)$ time, if the figure of merit is not the minimum separation but rather the minimum area of the circumscribing rectangle. []

In [DS], Theorems 1 and 3 are generalized to the case where wires may run along any finite set of diagonals of the grid. That is, the optimal separation may be calculated in $0(n)$ time and offsets in $0(n \log n)$ time. The most important special case occurs when wires are resticted to the eight 45° compass points, since many fabrication facilities handle rectangles in only these orientations. In fact, similar results hold even when wires are allowed to run on a grid finer than integer, and for certain classes of permitted wire shapes more general than straight lines, e.g., circles and parabolas.

References

[DS] Dolev, D. and A. Siegel, report in preparation.

[FP] Fischer, M. J. and M. S. Paterson, "Optimal tree layout," *Proc. Twelfth Annual ACM Symposium on the Theory of Computing*, pp. 177–189, 1980.

[J] Johannsen, D., "Bristle blocks: a silicon compiler,"

† In fact, we can use a 3λ grid if we alternate red and green (diffusion), but because of the capacitance inherent in green wires, there is good reason not to do so.

† This wire must be green if the horizontal grid is less than 10λ, and certain other combinations of horizontal and vertical grid sizes require that this wire be green, as well.

Caltech Conf. on VLSI, pp. 303–310, Jan., 1979. See also *Sixteenth Design Automation Proceedings*, pp. 310–313, June, 1979.

[L] LaPaugh, A. S, "A polynomial time algorithm for optimal routing around a rectangle," *Proc. Twenty-first Annual IEEE Symposium on Foundations of Computer Science*, pp. 282–293, 1980.

[MC] Mead, C. and L. Conway, *Introduction to VLSI Systems*, Addison Wesley, Reading, Mass.

[Sh] Shamos, M. I., "Geometry and statistics: problems at the interface," in *Algorithms and Complexity*, J. F. Traub, ed., Academic Press, 1976.

[St] Storer, J. A., "The node cost measure for embedding graphs on the planar grid," *Proc. Twelfth Annual ACM Symposium on the Theory of Computing*, pp. 201–210, 1980.

[T] Tompa, M., "An optimal solution to a wire-routing problem," *Proc. Twelfth Annual ACM Symposium on the Theory of Computing*, pp. 161–176, 1980.

[V] Valiant, L., "Universality considerations in VLSI circuits," CSR–54–80, Dept. of CS, Univ. of Edinburgh, 1980.