BME 194: Applied Circuits Lab 9 addendum

Kevin Karplus

March 4, 2013

This addendum adds more information to the original lab handout for Lab 9, the class-D power amplifier lab.

1 Design Goal

The design goal and constraints are essentially unchanged, though it will be sufficient to deliver 2W of power to the loudspeaker, not 10W.

2 Background

2.1 Real power

Unchanged.

2.2 Setting the power supply

You can use the gnuplot script `http://users.soe.ucsc.edu/~karplus/bme194/w13/lab-handouts/loudspeaker-low-p` `gnuplot` to help you choose a power-supply voltage that will deliver between 2W and 10W of power to the loudspeaker, using the detailed model of the loudspeaker and LC filter, rather than just the 8Ω estimate used in the initial handout.

It is important to remember that (for a fixed load) current will go up along with voltage, and so the real power will go up with the square of voltage. Also, the power computations in the gnuplot script are for sine waves, but the real power to the loud-speaker may be higher with other input signals (with square waves maximizing the power for a given power supply).

The handout suggested that a ±9V power supply could deliver 10W RMS in a square wave, so we don't want to exceed that voltage.

2.3 FETs as output stage

The biggest change in this addendum is a change in the output stage of the amplifier. Instead of tying the gates of the nFET and pFET together to make a single-input cMOS inverter, as suggested in the handout, you'll need to create separate control voltages for the two gates.

The simple inverter design has problems as the power supply voltages on the nFET and pFET sources increases, for two reasons:

- There are roughly three voltage ranges for the input to tied-together gates: below the nFET threshold (only the pFET is on), both FETs on, and above the pFET threshold (only the nFET is on). The nFET threshold is referenced to the nFET source (the lower power rail) and the pFET threshold is referenced to the pFET source (the upper power rail). Increasing the voltage difference between the power rails means that there is a wider range of gate voltages that cause both FETs to be on.

- The comparators that drive the gates have limited current capability, so as the power supply voltage increases, we need to use a larger pull-up resistor to get a low enough V_{OL} to turn off the nFET. But the gate capacitance is roughly constant, so as the power supply voltage is increased, the RC time

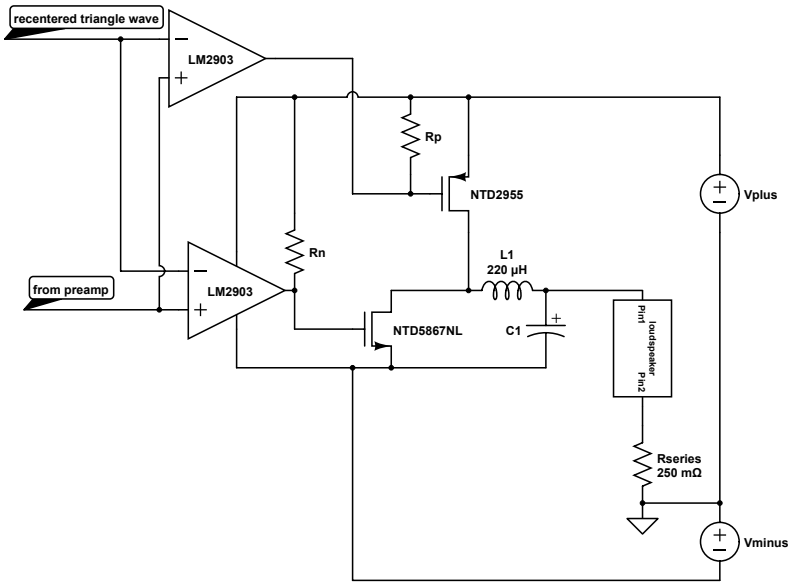

Figure 1: By having separate control signals for the gates of the nFET and pFET, we can arrange the signals to the gates so that the FETs are not simultaneously on. The basic idea is to make the gate signals have asymmetric rise and fall times, so that the FETs are turned off quickly, but turned on more slowly.

constants for the rise and time for the gates increases, which means that more time is spent in the region where both FETs are turned on.

By controlling the two gates separately, we can try to turn off one FET before turning on the other, reducing the wasted power that heats the FETs when both are on. Figure 1 shows one approach for doing this.

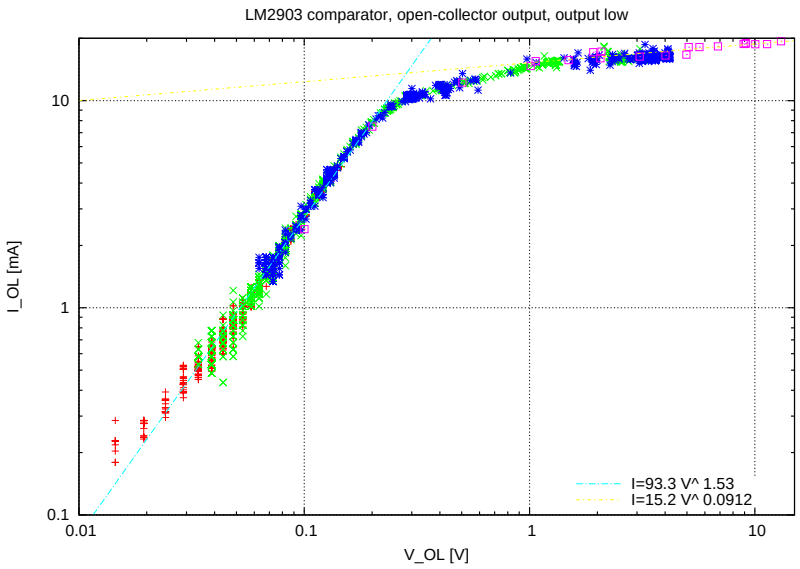

Figure 2: The output of the LM2903 comparator has an output current of around 15mA with $V_{OL} = 1$ and a saturation current around 18mA, even for $V_{OL} = 13v$, which is as high as I could measure at home. Note that I measured around 14–15mA at 1.5V, much more than the minimum spec of 6mA. It is often the case that minimum specs are much more conservative than typical values, to account for variation due to temperature, aging of parts, or variation in the manufacturing. The saturation current curve seems to depend somewhat on the voltage supplied to the LM2903 V_{CC} input, increasing somewhat with higher V_{CC}, but I did not investigate this carefully, due to lack of time.

2.4 LM2903 comparators

One warning (a mistake I made): be sure that your inputs to the LM2903 (coming from the preamplifier and the triangle-wave generator) remain between the power rails of the LM2903. If you use a separate power supply for the pre-amp, make sure its voltage is no higher than the voltages in the final-stage pwoer supply.

You will still need to understand the open-collector outputs of the LM2903 comparator, but instead of putting the two comparators in the package completely in parallel, you will connect the inputs together, but use one comparator to drive the pFET and one to drive the nFET.

To choose values for the pull-up resistors, we need to know how the output behaves. When the output is supposed to be high, the output-high voltage V_{OH} is the upper power rail and the gate capacitance is charged through the pull-up resistor. When the output is supposed to be low, the output-low voltage V_{OL} depends on the current through the LM2903 output transistor and the resulting IR drop across the pull-up resistor.

The spec sheets for the LM2903 do not give us good values for the output current vs. voltage characterisitic, so I tried measuring it with the same techniques we used in Lab 2 to characterize the electret microphone, using load resistors of various sizes (from 1kΩ down to 8.2Ω). The results are shown in Figure 2.

To a first approximation for output voltages higher than 1V, we can model the output as a current source with the saturation current of about $I_{sat} = 18$mA, and make a Thévenin equivalent for the pull-up resistor, power supply, and LM2903 output transistor:

- The output-low voltage V_{OL} would be the open-circuit voltage $V_{OL} = V_{oc} = 2V_{power} - I_{sat}R$, so for a power supply of ±7V and a pull-up resistance of 100Ω, $V_{OL} = 14V - 1.8V = 12.2V$. (That is

obviously too high an output-low voltage for us since it wouldn't turn off an nFET nor turn on a pFET, so that small a pull-up resistor would not work with that power-supply voltage.)

- The short-circuit current is just $I_{sc} = 2V_{power}/R - I_{sat}$.
- So the Thévenin equivalent is a voltage of $2V_{power} - I_{sat}R$ with a resistance of R.

Note that for both pulling up and pulling down, the equivalent resistance is R, so we can figure out rise and fall times by how many RC time constants it takes to reach a certain voltage.

If we start at V_0 and charge or discharge towards an endpoint of V_∞, then the charging curve is approximately $V(t) = V_\infty + (V_0 - V\infty)e^{-t/(RC)}$ and the time it takes to reach $V(t)$ is

$$t = RC \ln \frac{V_0 - V_\infty}{V(t) - V_\infty} \ . \tag{1}$$

This formula is a handy one for estimating how long it takes an FET to be turned off or on, though it is a rather crude approximation.

In sizing the pull-up resistors for the comparator outputs, you'll have the following considerations:

- The comparator driving the nFET must have a low enough output voltage when the output is supposed to be low (V_{OL}) that the nFET is turned completely off (less than 1.5V above the bottom power rail). This requires having a large enough pull-up resistor R_n that the voltage drop IR_n across the resistor is big enough. That is, $2V_{power} - I_{sat}R_n < 1.5$V. If the power voltages are increased, a larger IR drop is needed to keep the low output voltage below 1.5V above the lower power rail.
- The comparator driving the nFET must have a high enough output voltage when the output is supposed to be high (V_{OH}) to turn on the nFET (say, at least 3V above the bottom power rail). This is trivial to arrange, as long as the voltages on the power rails are big enough, as the V_{OH} of the pulled-up open-collector output is the upper power rail.
- The comparator driving the pFET must have a high enough V_{OH} that the pFET is turned completely off. This is also trivial to arrange, since there is no DC current flow, and V_{OH} is the upper power rail.
- The comparator driving the pFET must have a low enough V_{OL} that the pFET is turned on, say at least 4V below the upper power rail. This means that the pullup resistor R_p must be large enough that the IR_p drop is at least 4V, and preferably more. That is $I_{sat}R_p > 4$V.
- To make sure that we are getting fast rise times compared to our PWM frequency, we want $R_nC_n \ll T_{PWM}$ and $R_pC_p \ll T_{PWM}$, where T_{PWM} is the period of the triangle wave input to the comparator.
- We are interested in how long it takes the nFET and the pFET to turn on and off, and we can use the charging/discharging formula in Equation 1.
  - nFET on: V_{gs} starts at $V_0 = 2V_{power} - I_{sat}R_n$, rises to $V_\infty = 2V_{power}$ and we care when it gets bigger than $V_{nt} \approx 1.5$V.
  - nFET off: for V_{gs}, $V_0 = 2V_{power}$, $V_\infty = 2V_{power} - I_{sat}R_n$, and we care when it gets smaller than V_{nt}.
  - pFET on: for V_{gs}, $V_0 = 0$, $V_\infty = -I_{sat}R_p$, and we care when it gets lower than $V_{pt} \approx -2.8$V.
  - pFET off: $V_0 = -I_{sat}R_p$, $V_infty = 0$, and we care when it gets above V_{pt}.

```
set ylabel "Charge or discharge time [microsec]"
set xlabel "Pull-up resistance [ohm]"
set samples 10000

charge_time(r,c,V0,Vinf,Vth) = 1e6* r*c* log( (V0-Vinf) / (Vth-Vinf))

set xrange[100:4000]
set yrange [0.01:10]
set logscale x
set logscale y

set key top left

Vsupply=6 # power supply is +- Vsupply
Isat = 0.018    # saturation current of open-collector comparator

set title \
 sprintf("LM2903, +-%.3gV power, time to (dis)charge FET gates to threshold",\
         Vsupply)


# Threshold voltage(s) and capacitance for nFET
Vntsmall=1.5
Vntbig=2.5
Cn=675e-12

# Threshold voltage(s) and capacitance for pFET
Vptbig=-4.0
Vptsmall=-2.8
Cp=750e-12

plot \
     charge_time(x,Cn,2*Vsupply-x*Isat,2*Vsupply,Vntbig) title "nFET on big",\
     charge_time(x,Cn,2*Vsupply-x*Isat,2*Vsupply,Vntsmall) title "nFET on small",\
     charge_time(x,Cn,2*Vsupply,2*Vsupply-x*Isat,Vntbig) title "nFET off big",\
     charge_time(x,Cn,2*Vsupply,2*Vsupply-x*Isat,Vntsmall) title "nFET off big",\
     charge_time(x,Cp,0,-x*Isat,Vptbig) title "pFET on big",\
     charge_time(x,Cp,0,-x*Isat,Vptsmall) lt 8  title "pFET on small",\
     charge_time(x,Cp,-x*Isat,0,Vptbig) title "pFET off big", \
     charge_time(x,Cp,-x*Isat,0,Vptsmall) title "pFET off small"
```

Figure 3: Gnuplot script to plot the time to charge or discharge an FET gate to a particular threshold. The script is available at `http://users.soe.ucsc.edu/~karplus/bme194/w13/lab-handouts/charge-times.gnuplot`. The pFET is turned on and off much faster, because the pullup is to the power rail for the pFET source. You will have to adjust the supply voltage and decide which values to use for the threshold voltages. The results of running the script with the parameters shown here is in Figure 4.

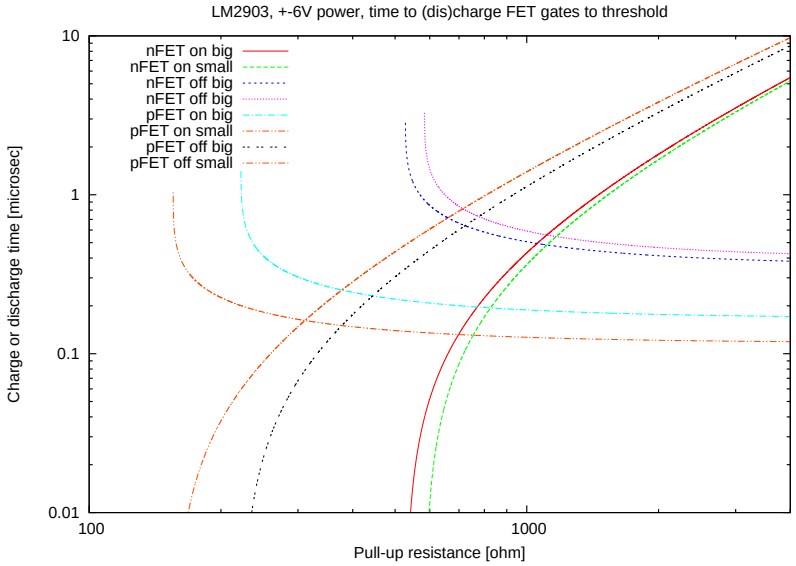

Figure 4: The result of running the gnuplot script of Figure 3. The resistance values where the times go asymptotically to 0 or ∞ are the absolute minimum values for the corresponding pull-up resistors.

The algebra gets a bit messy if you try to work this out, but it is easy to write a gnuplot script and plot the charge and discharge times for various parameter values (see Figure 3).

Note that you'll want R_p to be fairly small, to turn the pFET off quickly (but not so small that the pFET is not turned on when it is supposed to be) and a fairly large R_n so that the nFET is turned off quickly when it is supposed to be, but not so large that the nFET turn on time is more than a microsecond or two.

You might want R_p set so that the turn off and turn on times for the pFET are about the same and R_n set so that the turn on and turn off times for the nFET are about the same.

So we have several constraints on R_n and R_p, some of which depend on the gate capacitances and PWM frequency, some of which depend on the power supply voltages, and some of which depend on the maximum current through the LM2903 output transistors.

It is a good idea to write down all the constraints, to see if there are any reasonable solutions for R_n and R_p. The hardest thing to do is to estimate how the comparator output current varies with V_{OL}. The spec sheet for the LM2903 only specifies two points on the curve: ($V_{OL} = 1.5V, I_{OL} \geq 6mA$) and ($V_{OL} \leq 0.7V, I_{OL} = 4mA$). The first point is useful for setting R_n, since that is about the output voltage we want when the nFET is to be turned off. The spec sheet also has an absolute maximum of 20mA for I_O, and it would probably be a good idea to design for no more than about 18mA, which constrains R_p.

There is a fairly wide range of values possible for the R_n and R_p values, based on these constraints, but you probably want to use the smallest values that are consistent with the constraints, in order to keep the rise and fall times as short as possible.

2.5 Pulse-width modulation (PWM)

If you make the PWM frequency very high, it is difficult to make the rise and fall times for the gate voltages fast enough. If you make it too low, it is difficult to filter out the PWM pulses adequately without also filtering out some of your desired audio frequencies. Normally, a PWM frequency in the range 40kHz to 100kHz is chosen to blanace these conflicting constraints.

2.6 Inductive loads for PWM

No change from initial handout.

2.7 Output filter overview

No change from initial handout.

3 Pre-lab assignment

After choosing your PWM frequency and your power-supply voltage, go through the constraints on R_n and R_p to see if you can come up with resistances that meet all the constraints. If you pick too high a PWM frequency or too large a power-supply voltage, there may not be values that work.

I believe that the original specs can be met, but I've only tested the lab up to about ±7V for the FET power supply.

4 Parts, tools, and equipment needed

No change.

5 Procedures

Replace ±9V with whatever power supply voltage you use.

6 Demo and writeup

Unchanged.